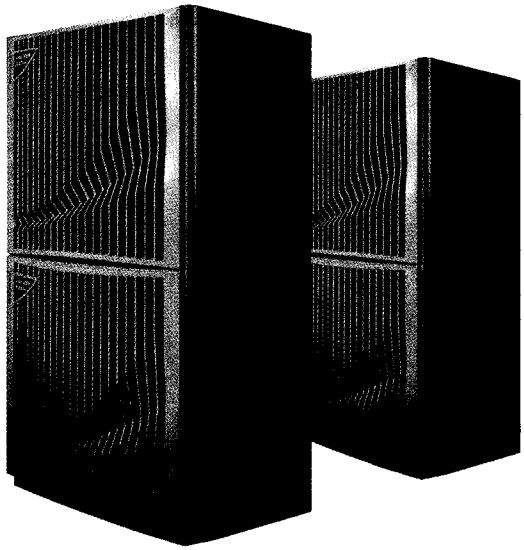
HEWLETT® PACKARD

S-Class and X-Class Servers



Exemplar Maintenance Guide

Second Edition

Exemplar Maintenance Guide S-Class and X-Class Servers

A4716-90023

Second Edition

August 1997

Hewlett-Packard Company
Convex Division
Richardson, Texas
United States of America

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Preface

Purpose and audience

This guide provides the system engineer with the information and procedures needed to remove and replace field replaceable units within the Exemplar S-Class and X-Class servers.

Scope

The information contained in this manual apply to the Exemplar S-Class and X-Class servers.

Notational conventions

This section discusses notational conventions used in this book.

Italic

In paragraph text, *italic* identifies new and important terms and titles of documents.

In command syntax diagrams, *italic* identifies variables that must be supplied by the user.

Bold

In paragraph text, **bold** identifies either equipment markings or actions that require an operator response.

Notes

This document presents notes in the following format.

Note

A Note highlights supplemental information.

Caution

A Caution highlights information necessary to avoid injury to personnel.

Warning

A Warning highlights information necessary to avoid damage to the system.

Associated documents

The following is a list of other documents that provide more details on the topics presented in this manual:

- Standard for the Protection of Electronic Computer Data Processing Equipment, (NFPA75) National Fire Protection Association
- EIA Standard RS-232-C, Electronic Industries Association
- Electrostatic Discharge Failures of Semiconductor Devices, Unger, B.A. 1981, Bell Laboratories

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Preliminary procedures

1

Overview

This chapter describes the tasks that are required prior to performing maintenance on the Exemplar S-Class and X-Class servers.

Power down the node

Perform the following steps to power down the node.

Step 1 Shut down the system with the `/etc/shutdown` command.

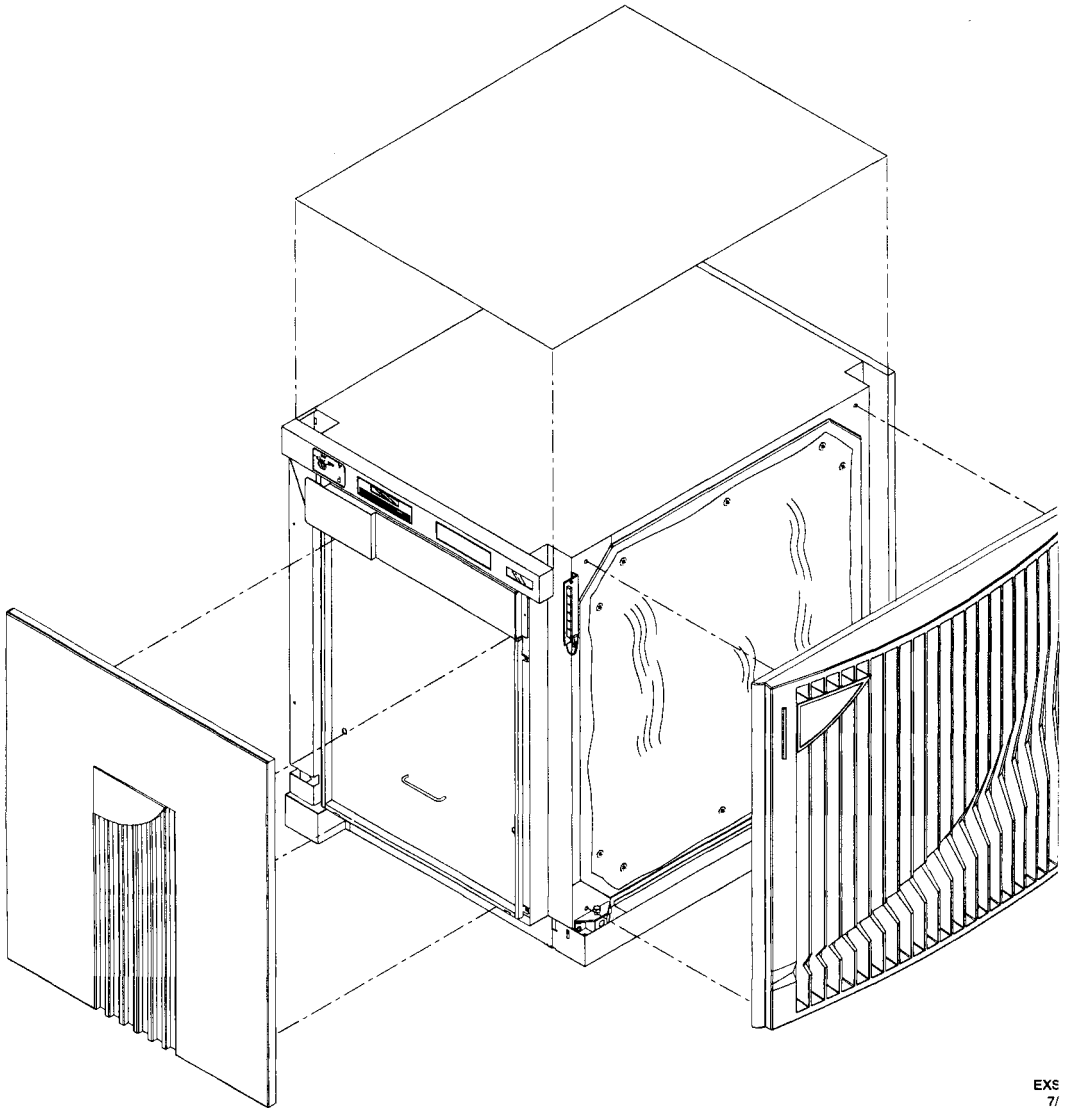
```
/etc/shutdown -h time
```

Step 2 Set the node keyswitch to **DC OFF**.

Skin removal

Determine which skins must be removed to gain access to the component to be removed or replaced. Skins are secured to the chassis by four force insertion pins. To remove a skin, grasp the skin on two sides and gently pull away from the chassis. Refer to Figure 1 for skin removal details.

Figure 1 Skin removal



EMI panel removal

Determine which EMI panel must be removed to gain access to the component to be removed or replaced.

Remove the EMI panels from the sides of the chassis. Refer to Figure 2 for EMI panel removal details.

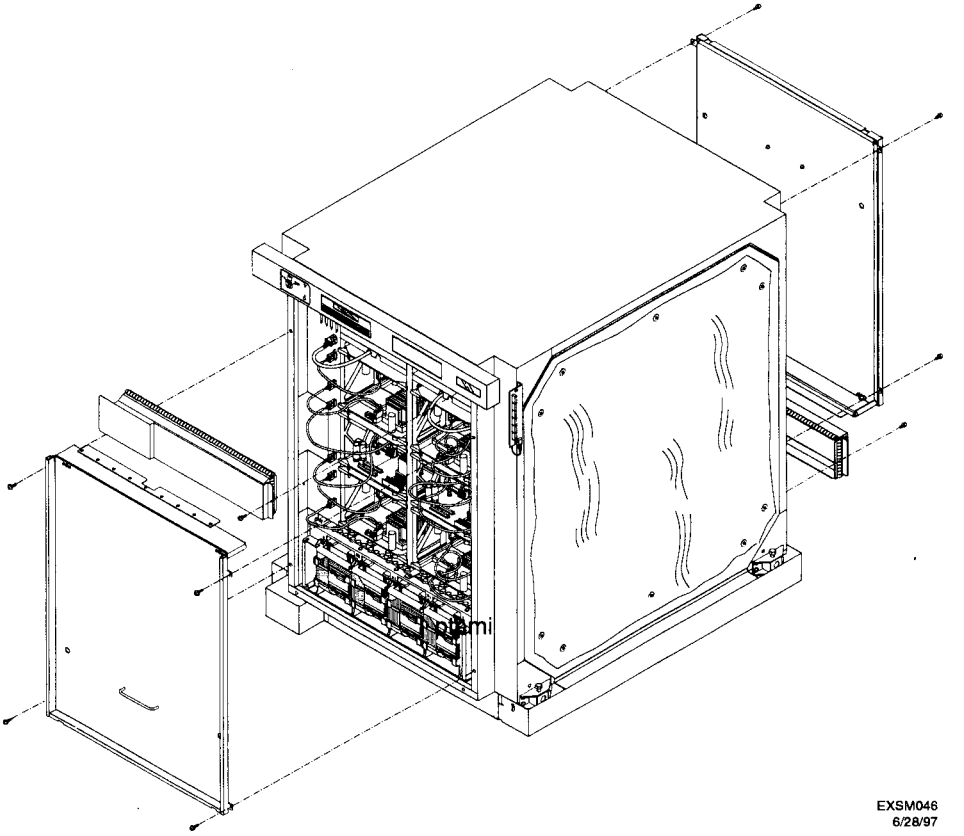
Step 1 Remove the screw securing the upper EMI panel.

Step 2 Lift the EMI cover away from the chassis.

Step 3 Remove the four screws securing the lower EMI panel.

Step 4 Remove the panel by pulling on the handle and maintaining leverage on the top of the panel to ensure that the panel does not tilt upward during removal.

Figure 2 EMI panel removal

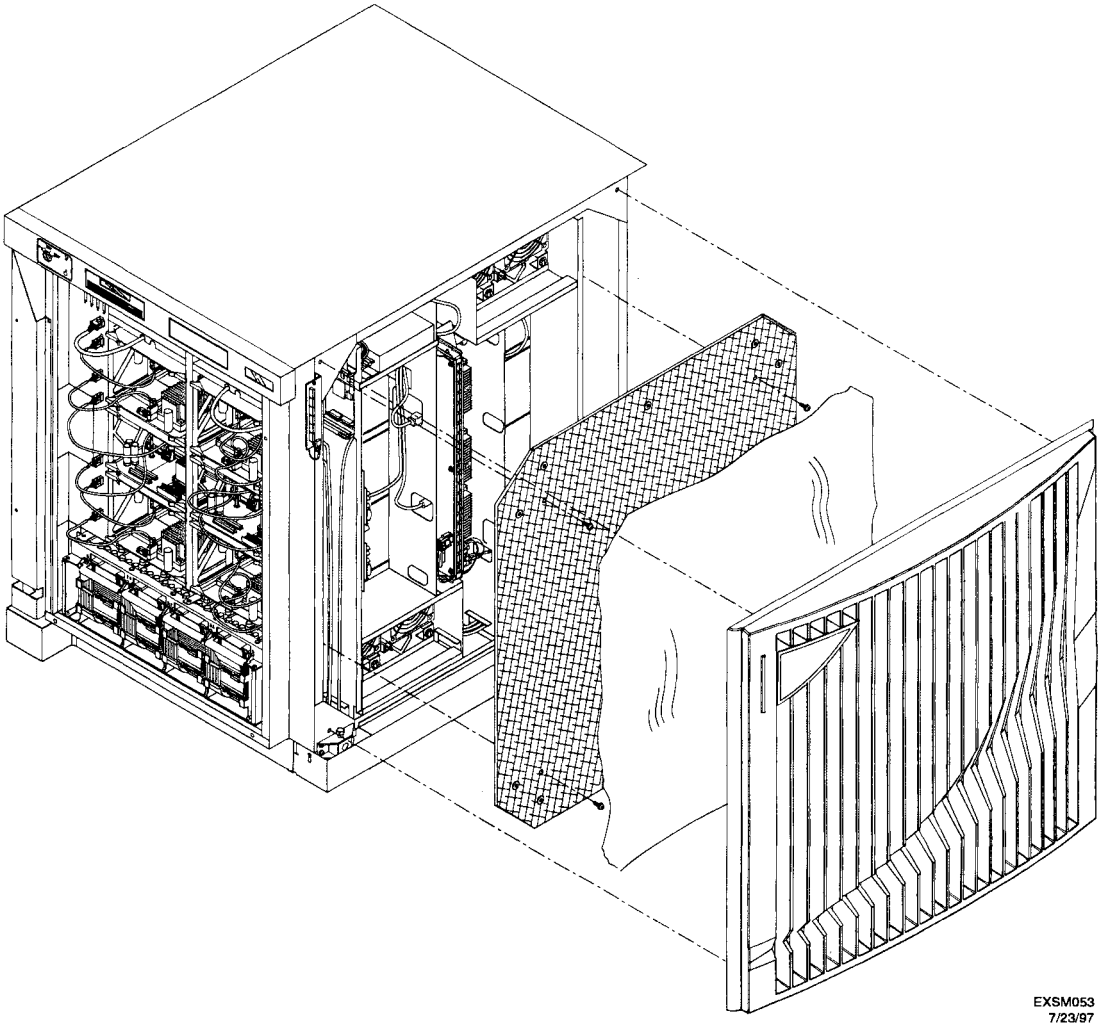


Remove the EMI panel from the front of the chassis. Refer to Figure 3 for front EMI panel details.

Step 1 Remove the filter by carefully pulling the velcro tabs loose.

Step 2 Remove the EMI panel by removing the screws securing it to the chassis.

Figure 3 Front EMI panel removal



Personal grounding

Direct discharge of a charged conductor or exposure to the static fields surrounding charged objects may cause electrostatic damage to electronic devices. The following procedure eliminates this type of damage.

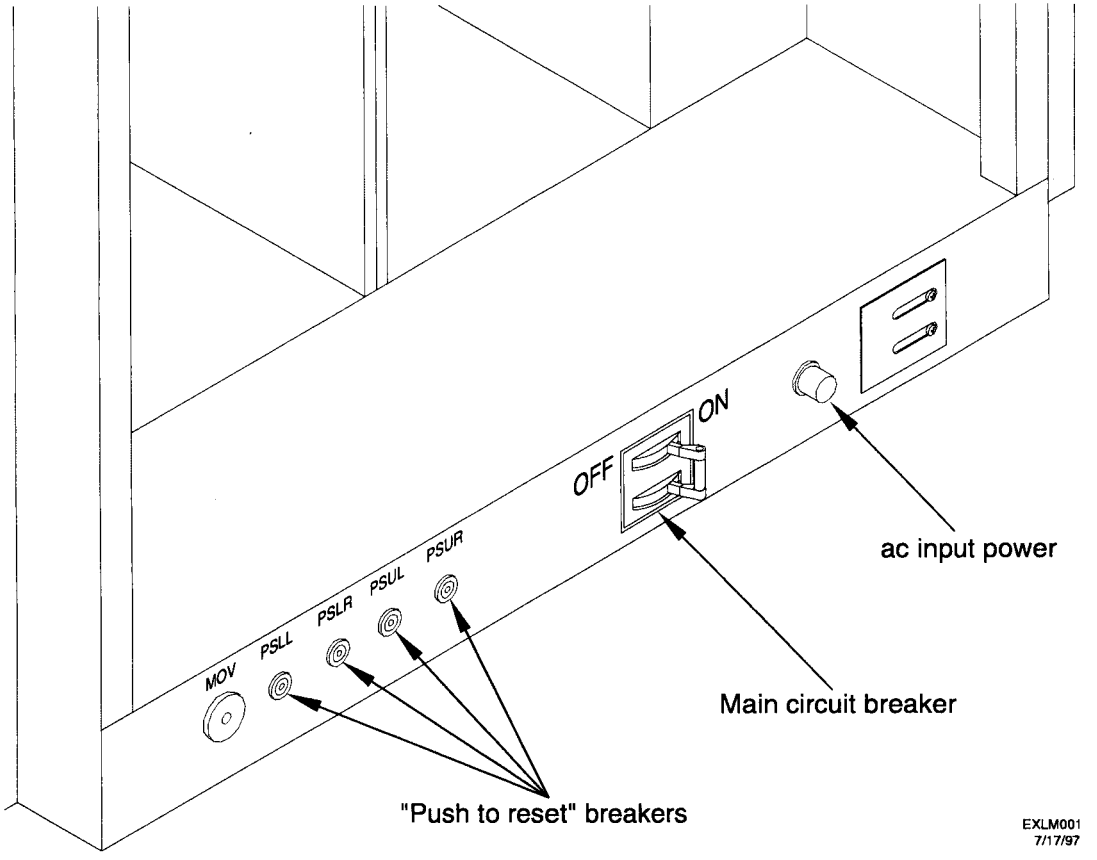
Step 1 Ground yourself to the node by wearing the wrist strap connected to a metal portion of the chassis.

Step 2 Position a static dissipating mat (grounded to node chassis) on the top of the node to set up a grounded work area.

Removing ac power

Remove ac power from the node, if required, by setting the main circuit breaker to **OFF**. Refer to Figure 4 for circuit breaker location.

Figure 4 Main circuit breaker location



Initialization

2

Overview

This chapter discusses initialization from when the breakers are turned on to when the Open Boot Program (OBP) completes its boot process. S-Class and X-Class servers are initialized as follows:

Step 1 Engage breakers.

Step 2 Power on server (key switch).

Step 3 Generate database.

Step 4 Monitor environment (core utilities board) (ECUB).

Step 5 Start Power-On Self Test (POST).

Step 6 Boot with Open Boot Prom (OBP).

Step 7 Load operating system (SPP-UX).

Major phases of system start-up

Table 1 lists the major phases of system start-up and indications of normal completion.

Table 1 Normal start-up

Sequence	Completion description
Connect line cord and power on	• ac power LED beside breaker is green. See Figure 7 on page 44.
Engage breaker	• Line delivers ac voltage to the 48V dc power supplies. • Power supply fans are on. • ac input LED on power supplies is amber. See Figure 8 on page 45.
Power on server (key switch)	• 48V is indicated by (dc) green LED on power supplies. See Figure 8 on page 45. • Four fans are on. • Core utility board power indicated by green light next to Keylock switch. • All system LEDs are lit (boards power up successfully).
Generate Database	• `ccmd` reads the system configuration and generates a database. • Message window displays: `INFO: Database generation is complete.`
Monitor environment (core utilities board) (ECUB)	• The power up sequence starts. • Fans and temperature sensors are monitored. • JTAG LEDs show normal activity (attention blinking). See Figure 13 on page 50.
Start Power-On Self Test (POST)	• POST initializes the processor and memory. • LCD panel displays Power-On Self Test (POST) sequencing after a few seconds. • Window of sppconsole shows POST messages (see following example).

Table 1 Normal start-up —**(continued)**

Sequence	Completion description
Boot with Open Boot Program (OBP)	Open Boot Program boots. Sppconsole displays OBP prompt. 0 (0,0) SN 20ffffff 1111 F111 --11 ----
Load operating system (SPP-UX)	Operating system is up. System is being used and active. 00 (0,0) CSN -000001 KIUU<ISUU< - - FU<UUUU Convex SPP-UX

The following is an example of correct output to the sppconsole window during POST initialization and OBP boot.

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
Probing CPUs.
Completing core SRAM initialization.
Initializing main memory.
   Probing memory: MB0L, MB1L, MB2R, MB3R, MB4L, MB5L, MB6R, MB7R
   Initializing MB0L........
   Initializing MB1L........
   Initializing MB2R........
   Initializing MB3R........
   Initializing MB4L........
   Initializing MB5L........
   Initializing MB6R........
   Initializing MB7R........
Booting OBP.
OPB Power-On Boot on [0:0]
SPP2000, OBP Release 3.0.2, compiled 97/01/07 11:55:13
16 CPUs, 4096 MB memory installed, 3 PCI units available.
Complex Serial Number: -1, Node Serial Number 2011255.
Network address 0:a0:d9:0:b0:77, OBP IP Number 15.99.111.150.
Using sppux boot-mode
[0:0] ok
```

Configuration

3

Overview

This chapter discusses the allowable configurations of Exemplar S-Class and X-Class servers.

- Minimum system configuration
- Order of configuration

Minimum configuration

Note

Airblockers are installed in pairs. Never install an airblocker adjacent to an installed board.

One way to check a failure is moving the failing processor, memory board, or I/O board (EIOB) to another slot and powering up the node to see if a failure follows. Taking a node to the minimum supported configuration for troubleshooting helps resolve many problems. Table 2 lists configurations.

Table 2 Minimum configuration

Number of processors	Number of agent ASICs	Number of memory boards	Total memory in MB	Number of EIOBs
4	2	2	256	1
	2	2	512	1
	2	2	1024	1
	2	4	2048	1
8	4	4	512	1 or 2
	4	4	1024	1 or 2
	4	4	2048	1 or 2
	4	4	4096	1 or 2
12	6	8	1024	1,2, or 3
	6	8	2038	1,2, or 3
	6	8	3072	1,2, or 3
	6	8	4096	1,2, or 3
16	8	8	1024	1,2,3, or 4
	8	8	2048	1,2,3, or 4
	8	8	3072	1,2,3, or 4
	8	8	4096	1,2,3, or 4

Order of configuration

Table 3 lists the order of configuration. See Figure 31 on page 153 for location of processors, memory boards, and I/O boards (EIOB).

Table 3 Order of configuration

Number of processors	Configure sequence	Processor location	EPAC location	Memory location	EIOB location
4	Seq 1	PB1L	P1R	MB0L	IOLR (IOB_1_5)
		PB1R	P5R	MB1L	
		PB5L			
		PB5R			
8	Seq2			MB6R	
	next 2 EMBs			MB7R	
	Seq 3	PB0L	P0L		
	next 4 EPBs	PB4L	P4L		
		PB0R			
		PB4R			
	Seq 4				IOLF (IOB_0_4)
	next optional EIOB				
	Seq5			MB2R	
	next 4 EMBs			MB3R	
				MB4L	
				MB5L	
12	Seq 6	PB2L	P2L		
	next 4 EPBs	PB6L	P6L		
		PB2R			
		PB6R			
	Seq 7				IORR (IOB_2_6)
	next optional EIOB				

Table 3 Order of configuration —**(continued)**

Number of processors	Configure sequence	Processor location	EPAC location	Memory location	EIOB location
16	Seq 8	PB3L	P3R		
	next 4 EPBs	PB7L	P7R		
		PB3R			
		PB7R			
	Seq 9				IORF (IOB_3_7)
	next option EIOB				

Troubleshooting utilities

4

Overview

This chapter discusses S-Class and X-Class server utilities for troubleshooting:

- `pce_util`—Resets and displays status of core utilities board
- `ds1620`—Reads and writes to temperature sensing
- `fix_boot_vector`—Determines process running
- `load_eprom`—Downloads core firmware
- `diag_version`—Displays version of diagnostics on the node
- `flash_info`—Displays contents of EEPROM
- `ver`—Retrieves teststation version

Utilities

The following sections describe utilities that diagnose problems. See the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* for more information on each utility, or use the `man` pages.

pce_util

This utility monitors and manipulates environmental conditions:

- Displaying core utilities board (ECUB) LEDs
- Margining power and/or clock frequency
- Resetting the environmental errors

It cannot be used to turn power off or to display individual dc power levels.

With no options, `pce_util` displays the current clock, power, and environmental state for each node under test.

The power and clock set points are fixed in hardware and cannot be changed with this utility.

The `pce_util` utility normally returns a zero value, even if some voltages or temperatures are out of tolerance. If a serious error occurs, `pce_util` returns a nonzero value.

Follow the sequence below to check an environmental error.

Step 1 Power up the node and wait for the complete message to show in the teststation console window.

```
INFO: node id 0 was found
INFO: Database generation is complete
```

Step 2 Type `pce_util` to display the error code LEDs section.

```
sppuser> pce_util -n 0
pce_util:   new node list: 0
Complex name is Default_complex
Node Clocks          LEDS   @C U SHPT Supply 1 Supply 2 Supply 3 Supply 4
---- ------ ------------- ---- ------ -------- -------- -------- --------
 0   Normal     ATTN 0x68   28 1 0000 Nominal  Nominal  Nominal  Nominal
```

After a few minutes, the following code in the teststation console window will display.

```
INFO: Environmental Warning: 68
```

Step 3 Find the meaning of the displayed code by referring to Chapter 10, "ENRB Troubleshooting."

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `pce_util` utility.

To margin power enter:

```
                              sppuser> pce_util -n 0 -p 1 all
pce_util:   new node list: 0
Complex name is Default_complex
Node Clocks          LEDS   @C U SHPT Supply 1 Supply 2 Supply 3 Supply 4
---- ------ ------------- ---- ------ -------- -------- -------- --------
 0   Normal       0x00      27 1 0000 Lower    Lower    Lower    Lower
```

To margin clock frequency enter:

```
                              sppuser> pce_util -n 0 -c s u
pce_util:   new node list: 0
data is 1 to write clock
Complex name is Default_complex
Node Clocks          LEDS   @C U SHPT Supply 1 Supply 2 Supply 3 Supply 4
---- ------ ------------- ---- ------ -------- -------- -------- --------
 0   Upper        0x00      27 1 0000 Lower    Lower    Lower    Lower
```

To reset the environmental core utilities board LEDs, use the following commands:

```
                              sppuser> pce_util -n 0 -r 1
pce_util:   new node list: 0
Complex name is Default_complex
Node Clocks          LEDS   @C U SHPT Supply 1 Supply 2 Supply 3 Supply 4
---- ------ ------------- ---- ------ -------- -------- -------- --------
 0   Normal       0x00     23 1 0010 Nominal  Nominal  Nominal  Nominal

                              sppuser> pce_util -n 0 -r 0
pce_util:   new node list: 0
Complex name is Default_complex
Node Clocks          LEDS   @C U SHPT Supply 1 Supply 2 Supply 3 Supply 4
---- ------ ------------- ---- ------ -------- -------- -------- --------
 0   Normal       0x00     23 1 0000 Nominal  Nominal  Nominal  Nominal
```

ds1620

The `ds1620` utility reads from or writes to the temperature sensing device. This utility determines when the system should shut down due to an over-temperature condition.

Caution

Do not change factory set points. Possible damage to the system may result

Follow the sequence below to produce a list with a node number, the temperature, and the set points with a description:

Wait until the following message appears in the teststation window before continuing:

```
INFO: Database generation complete
```

Step 1 Determine the current node number, the temperature, and the set points values with the following command.

```
sppuser> /spp/bin/ds1620 -n 0
```

Step 2 Change the set points as needed.

The following example sets node 0 lower set points to 32.

```
sppuser> /spp/bin/ds1620 -n 0 -s l 32
```

The following example sets node 0 higher set points to 37.

```
sppuser> /spp/bin/ds1620 -n -0 -s h 37
```

fix_boot_vector.cbus

This script restores the four words at the beginning of NVRAM to point to POST. These four words are used by the ENTRY firmware to determine which process was executing last when a High Priority Machine Check (HPMC), TOC, or reset occurs.

If it is suspected that the boot vector has become corrupted, follow these steps.

Step 1 Verify the error by checking the LCD panel for the need to manually load the boot_vector.

```
Reload boot firmware - bad boot_vector
```

Step 2 Fix the boot_vector by powering off of the server and then powering on again.

Step 3 If the reset fails after power on, run `fix_boot_vector` as shown below.

```
sppuser> /spp/scripts/fix_boot_vector.cbus
```

Sometimes it may be necessary to reload the boot_vector in NVRAM. This could be necessary after a do_reset or power off reset, and the following is displayed in the OBP window.

```
[0:c] F 6: fp 0x008e0800: pmap_enter_internal+0x1f4(0, 0, 0, 0)
[0:c] F 8: fp 0x008e06c0: kmem_alloc_pages+0x52c(0, 0, 0, 0)
[0:c] F 9: fp 0x008e0600: kmem_alloc_wired+0xe8(0, 0, 0, 0)
[0:c] F10: fp 0x008e0540: zalloc_internal+0x764(0, 0, 0, 0)
[0:c] F11: fp 0x008e04c0: zalloc+0x10(0, 0, 0, 0)
[0:c] F12: fp 0x008e0440: kalloc+0x68(0, 0, 0, 0)
[0:c] F13: fp 0x008e03c0: rpcRserver_thread_int+0x40(0, 0, 0, 0)
[0:c] F14: fp 0x008e0340: thread_continue+0x4c(0, 0, 0, 0)
[0:c]      KERNEL CSWITCH NEW THREAD
[0:c]      isqh 0x0000000000000000   ioqh 0x0000000000000000
[0:c]      isqt 0x0000000000000000   ioqt 0x0000000000000000
[0:c]      sp   0x00000000008e0340   fp   0x0000000000000000
[0:c]      mrp  0x0000000000000000   rp   0x00000000001b2a80
[0:c] F15: fp 0x00000000: thread_continue(0, 0, 0, 0)
[+8 f2560208 00000208 0:c] SPP-UX_mk   5.0 L34 tentacle:/work27/OOW/ECN_5_0 [S
PP8_FAST]
uk-panic(520): node 0 cpu 12: runway_hpmc
panic: runway_hpmc() at ../../../spp/spp3/hpmc.c:618
```

load_eprom

This utility is used to load twelve separate areas of NVRAM on the core utility board (ECUB). It is mainly used to load the entry.pdc (Entry point for the Processor Dependent Code (PDC)) and obp.pdc (Open Boot Program) modules.

The `load_eprom` utility performs the following functions:

- It reads a raw binary file on the teststation.
- It erases the specified flash sector and verifies that the erase was successful. It retries if the erase fails.
- It scans and then downloads the contents of the binary in 4096-byte page increments, updating the screen for each page with the following:
  - A "w" during the write operation.
  - An "r" during the optional read operation.
  - A "v" during the optional verify operation.
  - A "." when the page is complete.
- It can read each page back for verification.
- It can read-verify a binary in the flash EEPROM and compare it to the binary on the teststation without performing the write operation.

As an example, entering the following reads the file /spp/firmware/post.fw and updates the POST section of flash EEPROM on the core utilities board (ECUB).

```
sppuser> load_eprom -n mu_0000 -j jtag.fw
```

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `load_eprom` utility.

diag_version

The `diag_version` utility displays the product name and the version of the current Exemplar Diagnostic package as shown below:

```
sppdsh$diag_version
Exemplar Diagnostics, Version 1.0.1.0
```

flash_info

flash_info is a utility that probes the contents of the EEPROM on the core utilities board and displays the product name, version number, author, and date that the product was built.

It needs only one argument, the node number of the core utilities board to be examined. If flash_info is used without an argument, the first node found (from ccmd) is the node queried.

Information about what is loaded in flash EEPROM can be obtained by executing flash_info in the sppuser window:

```
sppuser> /spp/firmware$flash_info
Node: 0

Program Name        Version             Date         Author
post                001.000.000.000     1996/10/10   mullins
cpu3000             001.000.000.000     1996/10/10   mullins
No version string
No version string
No version string
test_controller     001.000.000.000     1996/10/10   mullins
mem3000             001.000.000.000     1996/10/10   blair
arch3000            001.000.000.000     1996/10/10   mullins
intra3000           001.000.000.000     1996/10/10   mullins
No version string
io3000              001.000.000.000     1996/10/10   mullins
```

ver

ver is a teststation version retriever utility. It is used to read and display the version information built into each diagnostic product. Its usage is:

ver *file*

ver searches the specified file for a version string and extracts and displays the version and date stamp, as shown in the following example:

```
sppuser> ver test_controller
PDC test_controller 001.004.000.017 1997/03/12 15:06:12 blair
```

Diagnostic tools

5

Overview

This chapter discusses S-Class and X-Class server scan and diagnostic tools. The `est` (Excalibur Scan Test) is usually run first, and, if it fails to find the problem, the diagnostic tests within `cxtest` can help isolate the problem.

- Scan Tools
  - `est`—Scans hardware (Excalibur Scan Test)
  - `jf-node_info`—Displays node information
- Test controller utility invoked by `cxtest`
  - `mem3000`—Tests memory functionality
  - `io3000`—Tests I/O functionality
  - `intra3000`—Tests memory functionality for multinode (single node)
  - `inter3000`—Tests memory functionality for multinode (minimum 2 nodes)
  - `arch3000`—Tests architecture functionality
  - `cpu3000`—Tests processor functionality
- System Exerciser (`sx`)—Tests for stress and stability

Excalibur scan test (est)

The Excalibur Scan Test (est) is a diagnostic utility that uses the system scan hardware making it possible to perform connectivity tests and to test gate array internals. The est utility runs on the teststation and sends scan instructions to a given node via ethernet. The features of est are summarized below

- est can be used to find scan rings errors and to locate bent connector pins, socket problems, (dc and ac connectivity) and bad gate arrays. Refer to the tables and examples below for each type of scan ring and its associated failure.

Note

Many I/O failures can be found using est; however, only the connections from the PCI-bus interface controller (EPIC) to the processor agent chip (EPAC) and the internal array registers are tested. est does not test the EPIC to the PCI cards or the cables so the io3000 subtests are required.

- est is started on the teststation and is located in /spp/bin/est. The user has the option of either starting up a user interface or having the est utility run a script.
- est works on one node at a time by sending scan instructions and data and receiving the results over the diagnostic ethernet connection.

Note

Do not run other diagnostics while est is running. est must communicate closely with the core utilities board.

Do not run the operating system while est is moving data through the scan rings.

Running `est`

This section explains how to run `est` and how to interpret errors.

Step 1 In the teststation console, type the following to load `est`.

```
sppuser> cd /spp/est
sppuser> est 0
Excalibur Scan Test 001.000.001.000 1997/01/22 11:20:116 Steven Terry
.....................................
.........
```

Step 2 When the main menu comes up, choose one of these options:

```
General EST Tests:
c ...compare id's to config file
r ...board level scan tests (return)
d ...board level dc tests (return)
a ...board level ac tests (return)
g [options] [file] ... gate array tests
Special Scan Tests:
b ...bypass/id test
i ...print id's found in design
EST options:
F ...set option & debug flags
q ...quit nicely, ask first
qq ..quit nicely, don't ask
Q ...quit, not so nice
h ...print this help message
v ...print EST version info
!cmd ...send the command to UNIX
>>
```

Step 3 Select the `r` *ring_number* option to display the following:

```
>> r 21 (in this case board level scan is selected)
Ring Test:
  Ring: 21
    Bypass
      Pattern 0xaaaa passed
      Pattern 0x5555 passed
      Pattern 0xffff passed
      Pattern 0x0000 passed
      Pattern 0x3333 passed
      Pattern 0xcafe passed
    Id
      Pattern 0xaaaa passed
      Pattern 0x5555 passed
      Pattern 0xffff passed
      Pattern 0x0000 passed
      Pattern 0x3333 passed
      Pattern 0xcafe passed
    Boundary
      Pattern 0xaaaa passed
      Pattern 0x5555 passed
```

```
      Pattern 0xffff passed
      Pattern 0x0000 passed
      Pattern 0x3333 passed
      Pattern 0xcafe passed
    Internal
      Pattern 0xaaaa passed
      Pattern 0x5555 passed
      Pattern 0xffff passed
      Pattern 0x0000 passed
      Pattern 0x3333 passed
      Pattern 0xcafe passed
Passed
```

If a test passes, the following displays.

```
PASSED or 0 ERRORS
```

Step 4 Select the `d` option to display the following if an error occurs:

```
>> d
```

```
DC Connectivity...
   SRAM64|pb21(6) Z055N9|42|actual: 0|expected:1
     wire: DATA041
       SRAM64|pb21(6) Z055N9|DQA6|6L
       UCHIP|pb21(6) U039P7|DCD041|AA31
```

The following example shows `est` failing on an SRAM on a processor board:

```
DC Connectivity...
   UCHIP|pb21(6) U039P7|536|actual:0|expected:1
     wire: R04DAT7
       EPAC|enrb(1) U022E3|R00_DAT[7]|G26
       UCHIP|pb21(6) U039P7|ADDRDATA7|C27
```

Step 5 Consult Table 4 through Table 7 for the possible cause if the test fails. Processor and memory board locations are stamped on the node chassis. The reference designator location is stamped on the node routing board.

If the test fails, information is supplied showing source part location, destination part location, and pin numbers. Expected and actual bit values, signal names, and in some cases pattern numbers are also shown.

For processor board (EPB) related scan rings refer to Table 4. Processor board locations are illustrated in Figure 37 on page 160.

Table 4 EPB scan rings

Scan Ring	Processor board location	CPU#	Reference designator location for related processor agent chip (EPAC)	EPAC	EIOB	EPIC
0	PB0L PB0R	0 1	U017Y3 Z017S8	P0L	Left front	0
1	PB1L PB1R	3 2	U061S1 Z061Z0	P1L	Left rear	1
2	PB2L PB2R	4 5	U061B7 Z061J6	P2R	Right rear	2
3	PB3L PB3R	7 6	U017H9 Z017C4	P3R	Right front	3
4	PB4L PB4R	8 9	U103Y3 Z013S8	P4L	Left front	4
5	PB5R PB5L	A B	Z147Z0 U147S1	P5L	Left rear	5
6	PB6L PB6R	C D	U147B7 Z147B7	P6R	Right rear	6
7	PB7R PB7L	E F	Z103C4 U103H9	P7R	Right front	7

For memory board (EMB) related scan rings see Table 5. See Figure 37 on page 160 for memory board locations.

Table 5 EMB scan rings

Scan Ring	Memory board location (left or right)	Reference designator location for related EMAC
8	MB0L	U007R0
9	MB1L	U093R0
10	MB2R	Z071R7
11	MB3R	Z157R7
12	MB4R	U071K0
13	MB5L	U157K0

Table 5 EMB scan rings —(continued)

Scan Ring	Memory board location (left or right)	Reference designator location for related EMAC
14	MB6R	Z007K7
15	MB7R	Z093K7

For PCI-bus interface controller (EPIC) related scan rings see Table 6.

Table 6 EPIC scan rings

Scan Ring	PCI-Bus Interface Controller Device location	Reference designator location for related EPIC
16	EPIC0 (left front) EPIC4 (left front)	IOLF - U157AA1
17	EPIC1 (left rear) EPIC5 (left rear)	IOLR - U071AA1
18	EPIC2 (right rear) EPIC6 (right rear)	IORR -Z071A6
19	EPIC3 (right rear) EPIC7 (right rear)	IORF - Z157A6

For routing attachment chip (ERAC), processor utilities chip (EPUC), and monitoring utilities chip (EMUC) related scan rings see Table 7.

Table 7 Other scan rings

Scan ring	ERAC (left or right), EPUC, or EMUC device
20	R0L R2R
21	R3R R1L
22	EPUC EMUC

jf_node_info

This utility displays the IP address, UDP port and JTAG firmware version string for each node in a complex.

```
sppdsh$ jf_node_info -e -c

Ethernet Address     IP Address                          UDP Port
------------------   -------------------------------     -----------------
00:a0:d9:00:ad:bd    15.99.11.100                        0x089a (2202)
                     jtag 1.1.0.0 1996/10/14             10:58:42 mullins
                     jtag_core 1.1.0.0 1996/10/14        10:58:42 mullins
```

Test controller utility

The test controller is an EEPROM-based utility that provides the environment for executing the offline diagnostic tests in two basic operational modes.

- Standalone mode—Invokes the test controller and uses test parameter inputs provided by test scripts or the cxtest (GUI) mode.
- Interactive mode—Allows user to select processors, select subtests to run, and examine error information.

Standalone mode

Below is an example when the test controller is invoked by `cxtest` in stand-alone mode using the command line interface.

All options are covered in the man page for `cxtest`. On the teststation enter:

```
sppuser> man cxtest
```

For the `cxtest` (GUI mode) consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

Step 1 In the teststation window, set the mode of the test controller to standalone mode and reset the system by typing the following:

```
/spp/scripts/tc_standalone
do_reset
```

Below is a result in the sppuser window when booted in standalone mode.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
Running in Standalone Mode.
```

Step 2 Utilize the command line options of `cxtest` to check memory that failed with subtests 110, 120, and 150 through 170.

```
cxtest -mem -pa5 7 -pa6 0 -s 110,120,150-170 -c 4-6
```

Interactive mode

Below is an example when the test controller is invoked by in interactive mode using the menu interface.

Step 1 In the teststation window, set the mode of the test controller to interactive mode and reset the system by typing the following:

```
sppuser> /spp/scripts/tc_interactive
sppuser> do_reset
```

Below is the result in the sppuser window when booted in interactive mode

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
    0=Quit Test Controller
    1=Begin Test Controller Execution
    2=Halt Test Controller Execution
    3=Resume Test Controller Execution
    4=Switch CPU
    5=POST Boot selection
    6=Execution Mode Selection
    7=Global Parameter Display
    8=CPU Summary Display
    9=Display CPU Errors
    A=Test Selection Menu
    B=Test Configuration Menu
    C=Debugging Menu
    D=Display Revision
Enter command:
```

Step 2 In the teststation window, set up the test controller for selection of a particular test by entering the command:

```
Enter command: A
```

Step 3 From the Test Selection Menu, enter the test number to run:

```
    1=Memory test
    2=Archetecture Features test
    3=Intra-Node Coherency test
    4=Inter-node Coherency test
    5=I/O test
    6=CPU Selftests
Please enter number of test: 5
```

Test controller subtests

In the following sections and chapters, each subtest number is summarized. Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the test controller.

mem3000

The `mem3000` subtest tests functionality of the memory subsystem. You can select it from the Test Selection Menu in the sppuser window. For descriptions and various features of a test, type `man` *test* in a teststation window. For an example of `mem3000`, see Chapter 11, "Memory board errors."

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `mem3000` utility.

io3000

The io3000 subtest tests functionality of the I/O subsystem. You can select it from the Test Selection Menu in the sppuser window.

Note

Many I/O failures can be found using est; however, only the connections from the PCI-bus interface controller (EPIC) to the processor agent chip (EPAC) and the internal array registers are tested. est does not test the EPIC to the PCI cards or the cables so the io3000 subtests are required.

For descriptions and various features of a test, type man *test* in a sppuser window. For an example of io3000 in interactive mode see below.

Step 1 In the sppuser window, set the mode of the test controller to interactive mode, and reset the system.

```
sppuser> /spp/scripts/tc_interactive
sppuser> do_reset
```

The following illustrates the result in the sppuser when booted in interactive mode.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command:
```

Step 2 Use the sppuser window again to set up the test controller for selection of a particular test by entering the command:

```
Enter command: A
```

Step 3 From the Test Selection Menu, enter the I/O test number:

```
    1=Memory test
    2=Archetecture Features test
    3=Intra-Node Coherency test
    4=Inter-node Coherency test
    5=I/O test
    6=CPU Selftests
Please enter number of test: 5
```

Step 4 Return to the Main Menu.

```
Enter command: 0
```

Step 5 Select the Test Configuration Submenu.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: B
```

Step 6 In the Test Configuration Submenu, select item 4.

```
Test Configuration Menu
   0=Return to Main Menu       9=Display Test Parameters
   1=Display Classes           A=Hardware Selection Menu
   2=Display Subtest           B=Loop Enable
   3=Select Classes            C=Loop Count
   4=Select Subtests           D=Test Error Count
   5=Read All Test Parameters  E=Pause at Test Start
   6=Read One Test Parameter   F=Pause at Test End
   7=Write Test Parameter      G=Pause at Subtest Start
   8=Reset Parameters          H=Pause at Subtest End
Enter command: 4
```

Step 7 Enter the subtest or subtest range from the chart in the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

```
Enter the subtest number or subtest range: 100-300
```

Step 8 Return to the Main Menu.

```
Enter command: 0
```

Step 9 From the Main Menu, begin the Test Controller by selecting option 1.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
    0=Quit Test Controller
    1=Begin Test Controller Execution
    2=Halt Test Controller Execution
    3=Resume Test Controller Execution
    4=Switch CPU
    5=POST Boot selection
    6=Execution Mode Selection
    7=Global Parameter Display
    8=CPU Summary Display
    9=Display CPU Errors
    A=Test Selection Menu
    B=Test Configuration Menu
    C=Debugging Menu
    D=Display Revision
Enter command: 1
```

The sppuser window displays the following:

```
Execution Starting.
.............
.............
Execution Complete
```

The Main Menu comes up again after the test completes.

Step 10 To see the test results, select the CPU summary option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
    0=Quit Test Controller
    1=Begin Test Controller Execution
    2=Halt Test Controller Execution
    3=Resume Test Controller Execution
    4=Switch CPU
    5=POST Boot selection
    6=Execution Mode Selection
    7=Global Parameter Display
    8=CPU Summary Display
    9=Display CPU Errors
    A=Test Selection Menu
    B=Test Configuration Menu
    C=Debugging Menu
    D=Display Revision
Enter command: 8
```

This selection shows if the test passed or failed

```
CPU  STATE     FAIL      SUBTEST       TEST NAME
                COUNT

==   =====     =====     ======        ========

2    Failed    0         200           IO3000-EEPROM based IO tests
```

Step 11 To see how the test failed, select the Display CPU option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 9
```

This selection shows how the test failed.

```
Enter CPU [0-f]: 4

 Date/Time  hh:mm:ss   SUBTEST   Event      Error
  mm/dd/yy                      Code       Message

 =========  ========   =======   ========   ========

 03/03/97   14:06:55   310       80c43220   IOLF_B/fc010008/00e000000/00e00000f0c
                                             1000000
```

Step 12 To determine what error messages mean, refer to the `man` pages for `io3000` by cross-referencing the last two digits of the event code to the list of error code meanings. The error message

```
IOLF_B/fc010008/00e000000/00e00000f0c1000000
```

translates to

```
EPIC_name/address/act_val/exp_val
```

The exp_val shows that it is an EPIC CSR error.

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `io3000` utility.

intra3000

This is a single node test of mutinode global memory features. A single node is connected with the SCI cables, such that it appears to the diagnostics as a multinode server. These tests are grouped together in classes and cover intranode coherency tests, parallel intra-node coherency tests, strong ordering tests, and random tests. Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more detailed information.

inter3000

This is a true multinode test of multinode global memory features, and it requires at least 2 nodes. These tests are grouped together into classes that cover internode coherency, toroidal access chip (ETAC) and memory access chip (EMAC) errors, messaging and data copy, stress, and internode coherency parallel tests. See the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information.

arch3000

This is a test of various architectural features of the system. Included in the tests are CSRs, messaging, datamover, interrupts, semaphore operations, and CTI cache operations. These tests are grouped together in classes and are discussed in detail in the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

cpu3000

This is a processor test for S-Class and X-Class servers. `cpu3000` is used to verify the functionality of the processor module. The tests are grouped together in classes covering basic CPU tests, instruction cache RAM test, data cache RAM tests, and TLB RAM tests. Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on `cpu3000`.

Most CPU failures can be found using `est`; however, some require further investigation and require the `cpu3000` test. Refer to Chapter 12,"Processor errors" for an example.

System Exerciser (sx)

sx is a generic test driver used for stress testing and system stability verification on S-Class and X-Class servers. sx has both a graphical user interface (GUI) and a command-line interface. Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the sx utility.

System initialization faults

6

Overview

This chapter discusses general initialization failures between the time that the key switch is turned on and OBP completes its boot process.

- Major phases of system start-up
- Troubleshooting at initialization

Major phases of system start-up

Table 8 lists the major phases of system start-up and indications of normal completion. Locations of LEDs are shown in the figures of this section.

Table 8 Normal powerup

Sequence	Normal description
Connect line cord and power on	• ac power LED beside breaker is green. See Figure 7 on page 44.
Engage breaker	• Line delivers ac voltage to the 48V dc power supplies. • Power supply fans should be on at this point. • ac input LED on power supplies is amber. See Figure 8 on page 45.
Power on server (key switch)	• 48V is indicated by (dc) green LED on power supplies. See Figure 8 on page 45. • Four fans are on. • Core utility board power indicated by green light next to Keylock switch. • All system LEDs are lit (boards power up successfully).
Generate Database	• `ccmd` reads the system configuration and generates a database. • Message window shows: `INFO: Database generation is complete.`
Monitor environment (core utilities board) (ECUB)	• The power up sequence is started • Fans and temperature sensors are monitored. • JTAG LEDs show normal activity (attention blinking). See Figure 13 on page 50.
Start Power-On Self Test (POST)	• POST initializes the processor and memory. • LCD panel displays Power-On Self Test (POST) sequencing after a few seconds. • Window of sppconsole shows POST messages (see following example).

Table 8 Normal powerup —**(continued)**

Sequence	Normal description
Boot with Open Boot Program (OBP)	Open Boot Program boots. Sppconsole displays OBP prompt. 0 (0,0) SN 20ffffff 1111 F111 --11 ----
Load Operating System (SPP-UX OS)	Operating system is up. System is being used and active. 00 (0,0) CSN -000001 KIUU<ISUU< - - FU<UUUU Convex SPP-UX

The following is an example of correct output to the sppconsole window during POST initialization and OBP boot.

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
Probing CPUs.
Completing core SRAM initialization.
Initializing main memory.
   Probing memory: MB0L, MB1L, MB2R, MB3R, MB4L, MB5L, MB6R, MB7R
   Initializing MB0L........
   Initializing MB1L........
   Initializing MB2R........
   Initializing MB3R........
   Initializing MB4L........
   Initializing MB5L........
   Initializing MB6R........
   Initializing MB7R........
Booting OBP.
OPB Power-On Boot on [0:0]
SPP2000, OBP Release 3.0.2, compiled 97/01/07 11:55:13
16 CPUs, 4096 MB memory installed, 3 PCI units available.
Complex Serial Number: -1, Node Serial Number 2011255.
Network address 0:a0:d9:0:b0:77, OBP IP Number 15.99.111.150.
Using sppux boot-mode
[0:0] ok
```

Figure 5 Memory board (EMB) LEDs

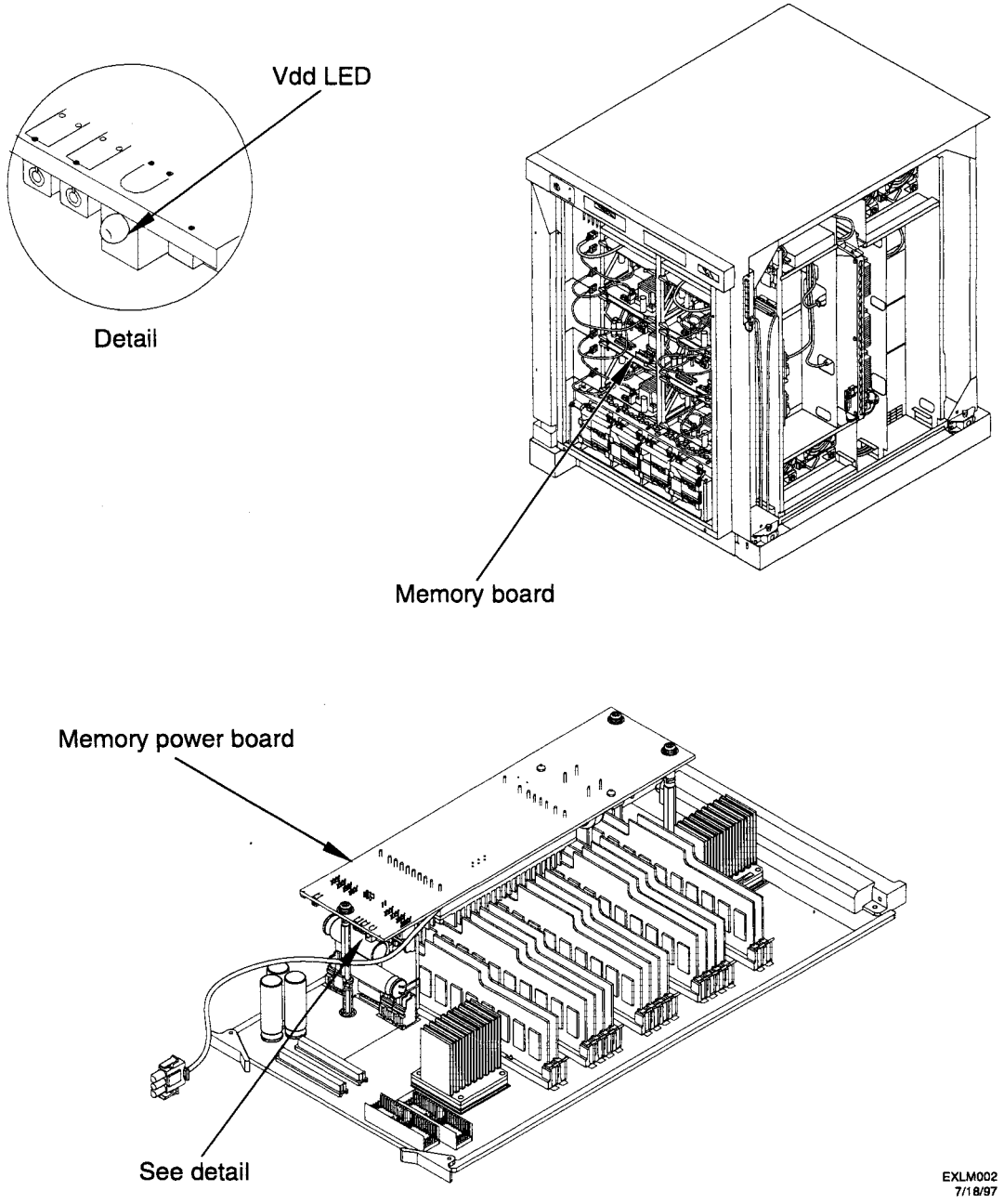


Figure 6 Processor board (EPB) LEDs

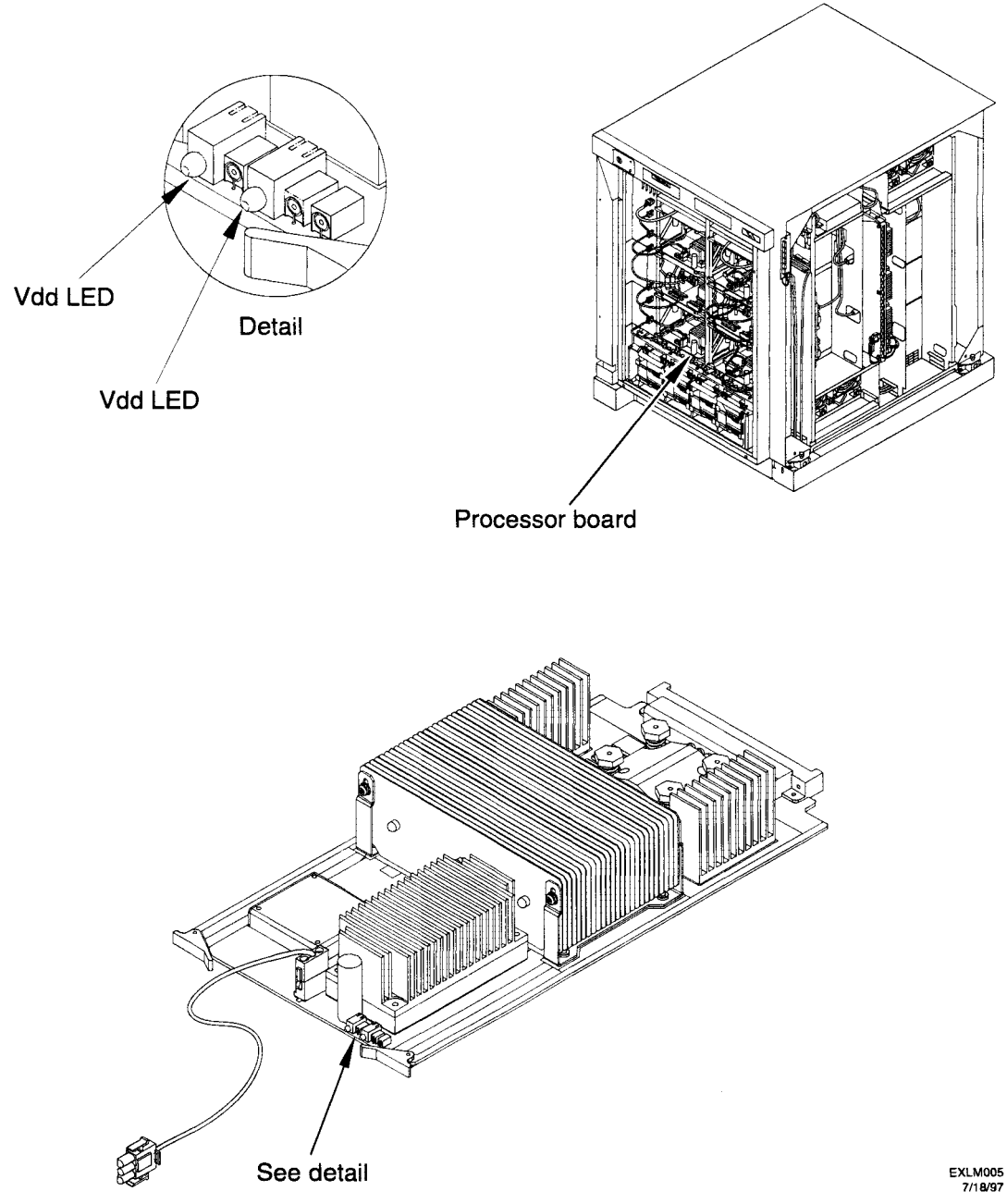


Figure 7 Breaker and ac power LEDs

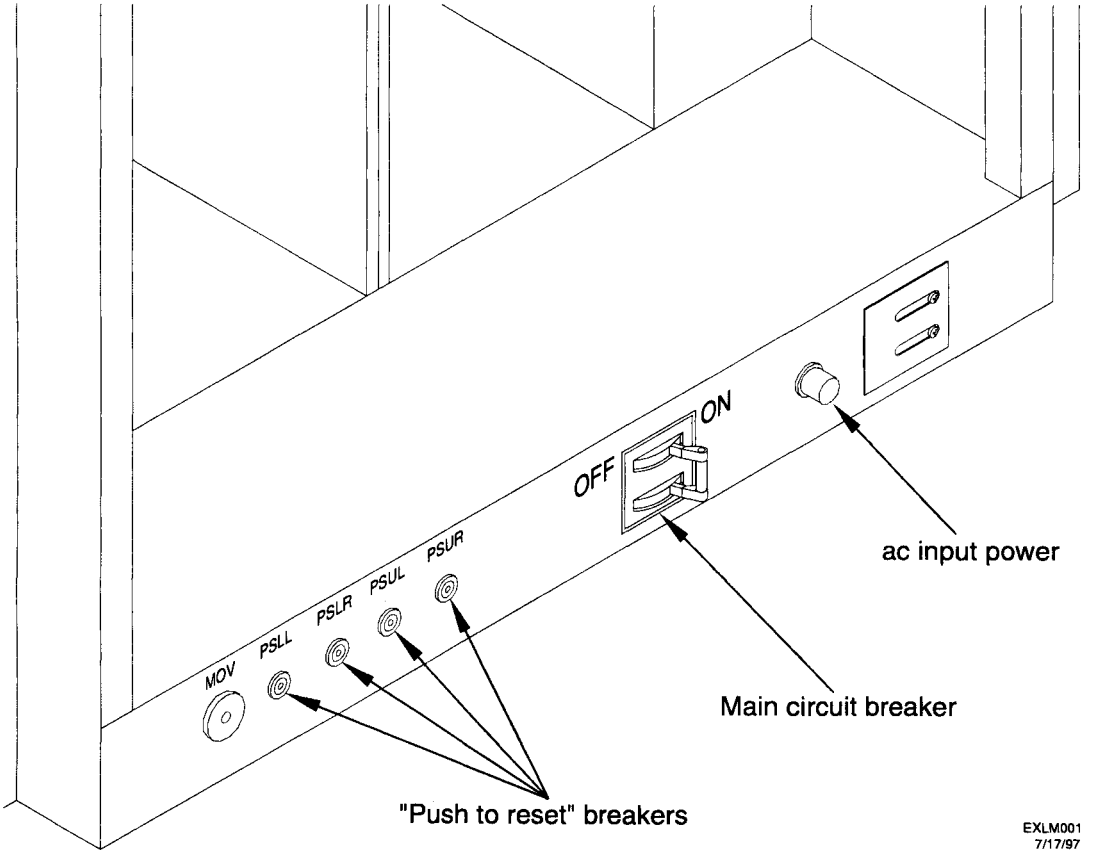


Figure 8 Power supply LEDs

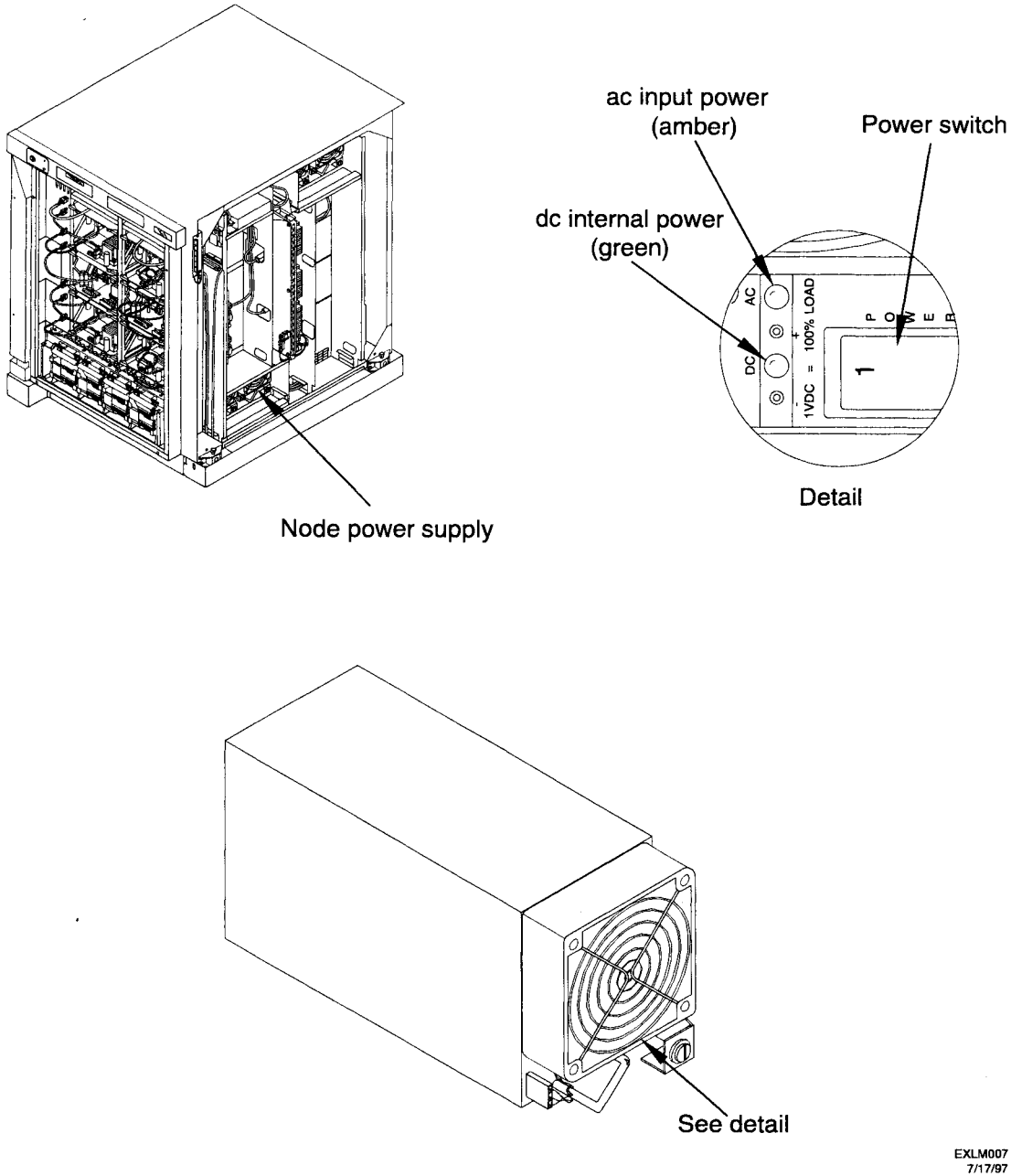


Figure 9 SE TO DIFF LEDs

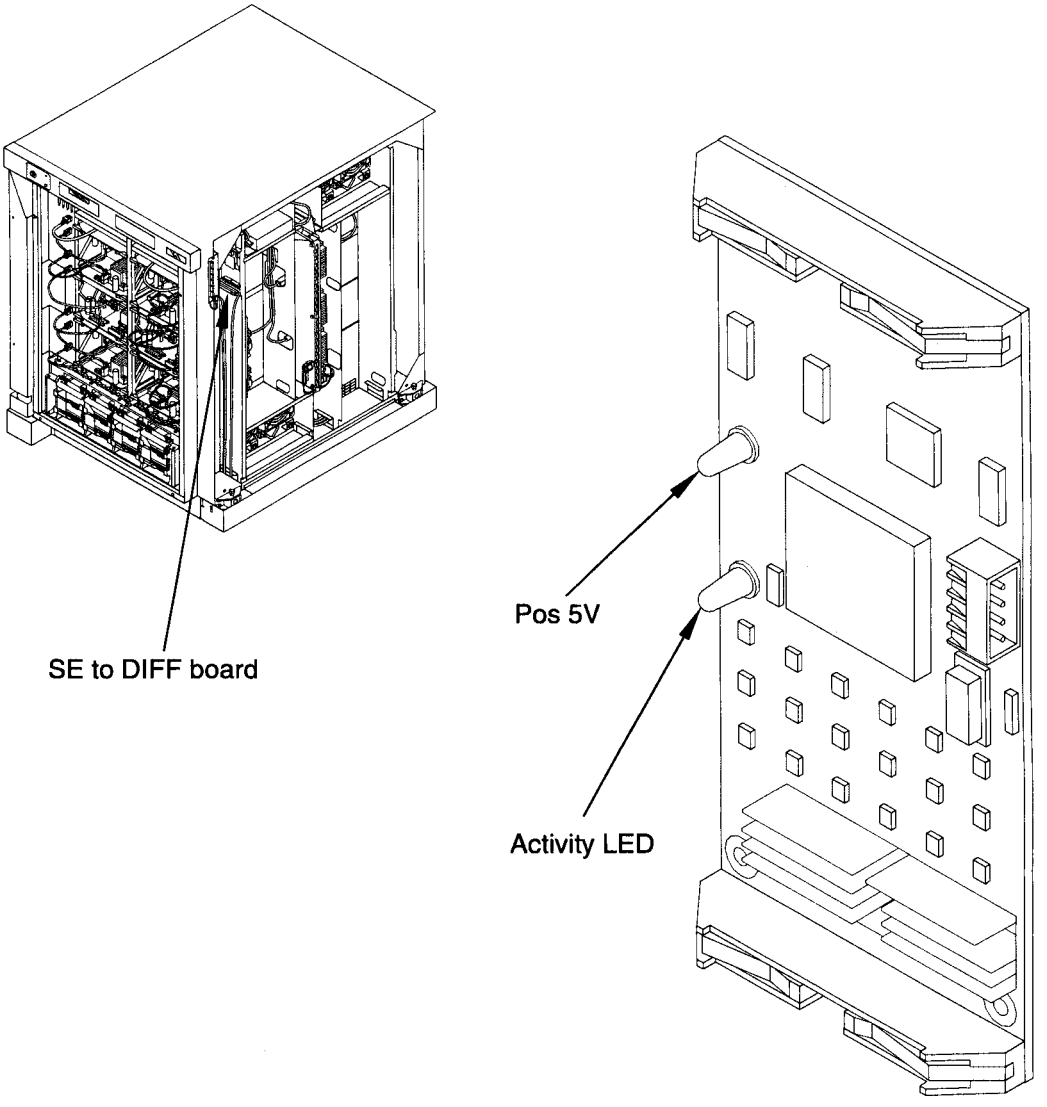


Figure 10 Embedded disk power board (EEDPB2) LEDs

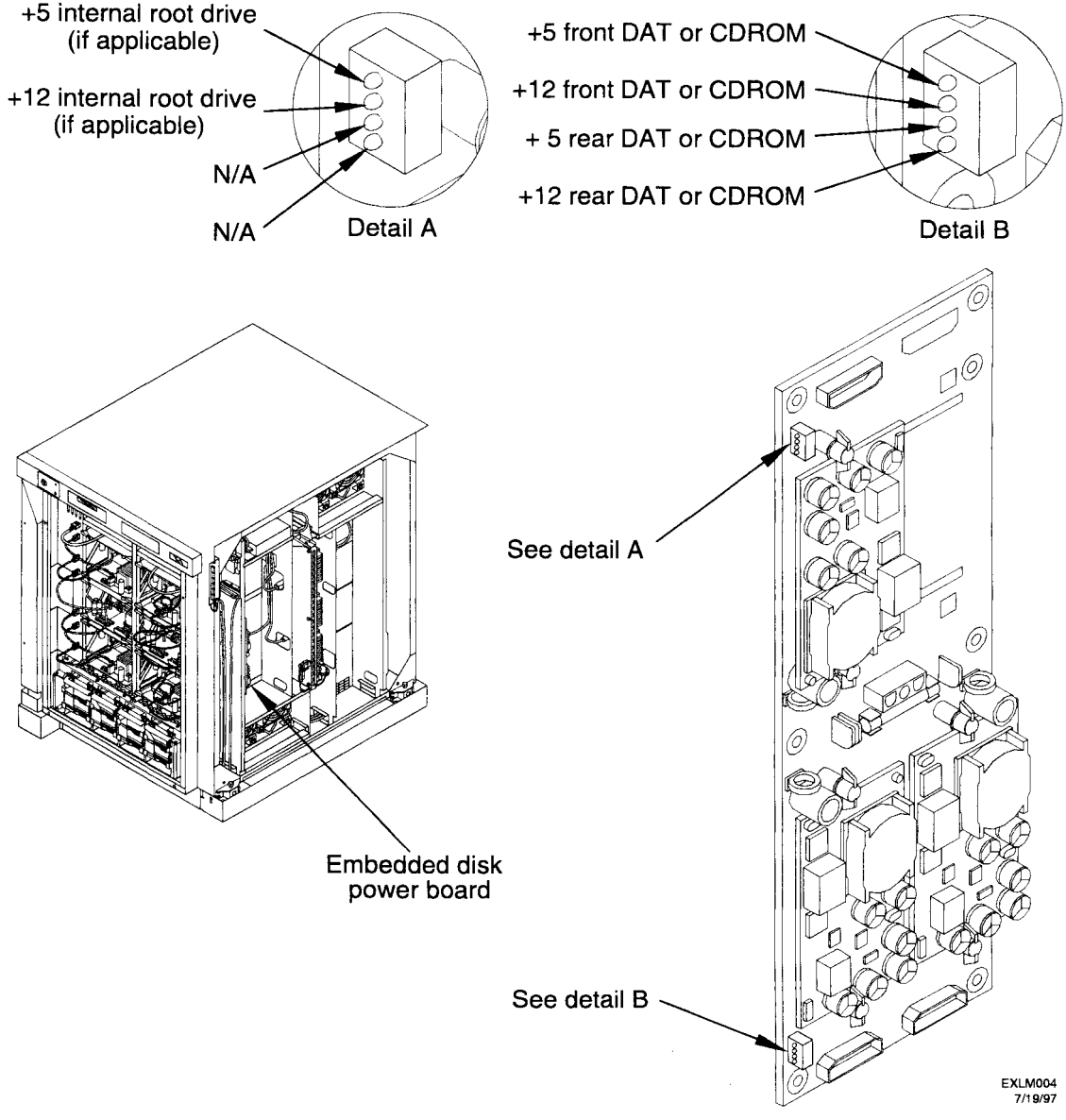


Figure 11 I/O board (EIOB) LEDs

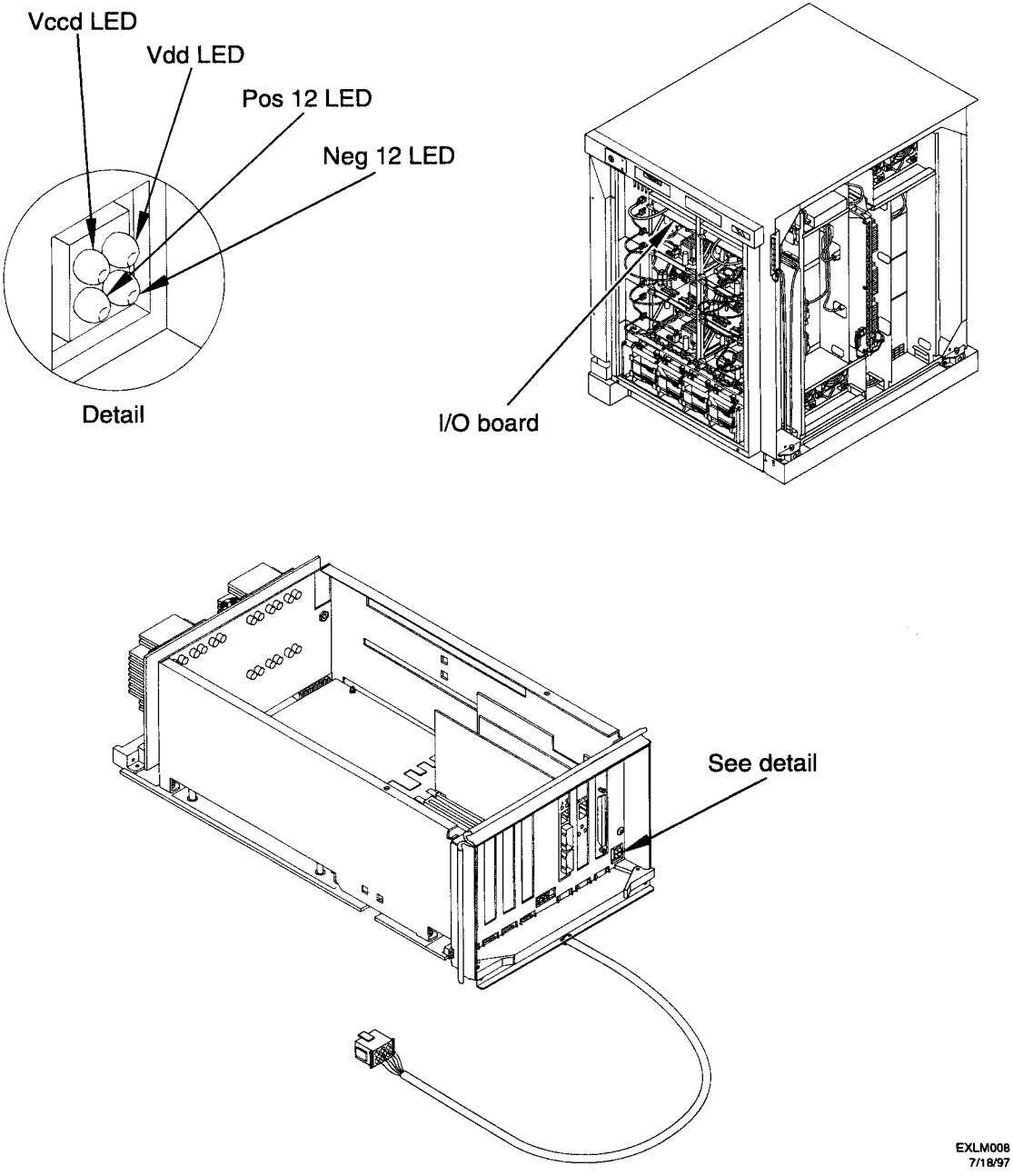


Figure 12 Node routing board power board (ENRBPB) LEDs

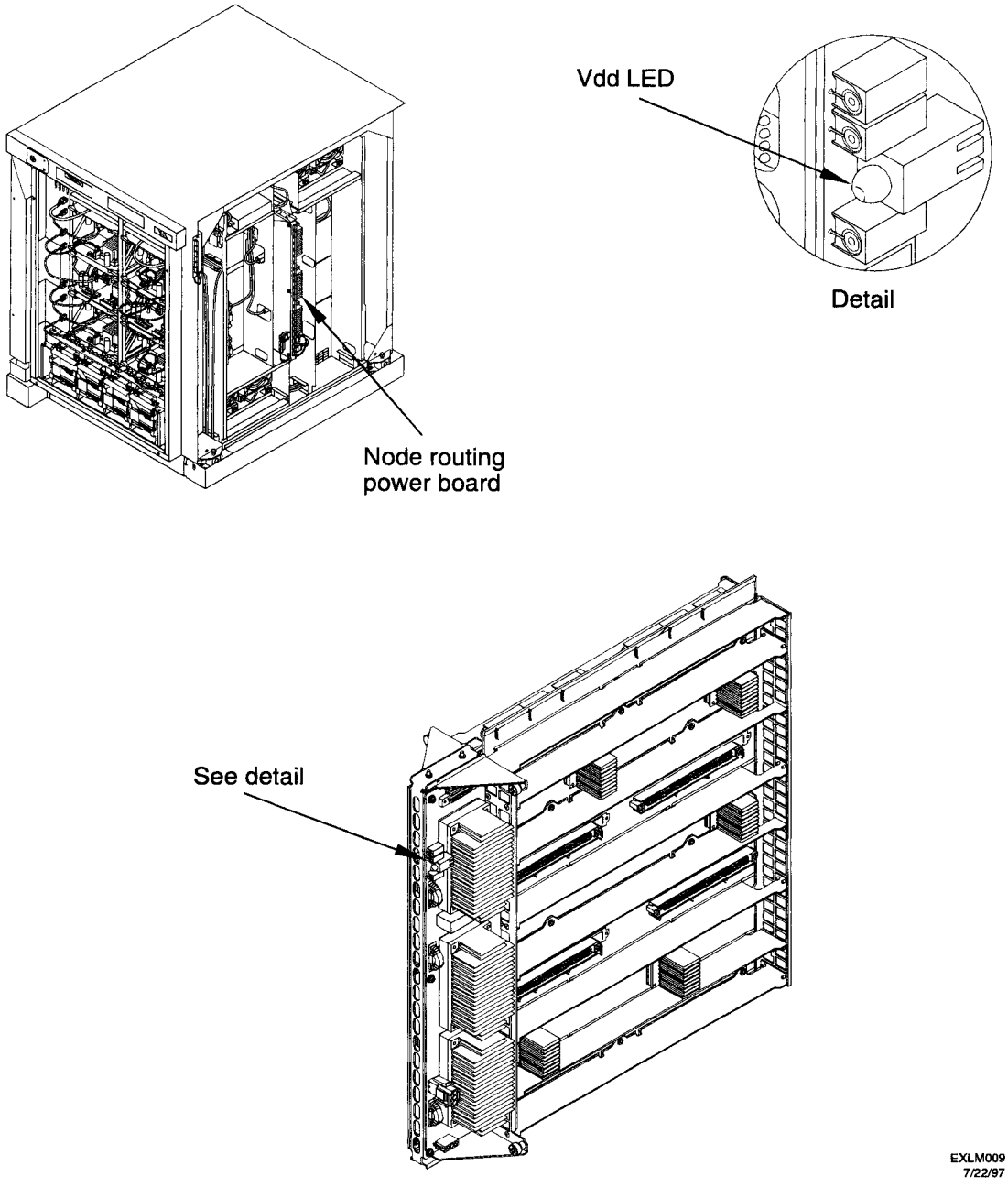
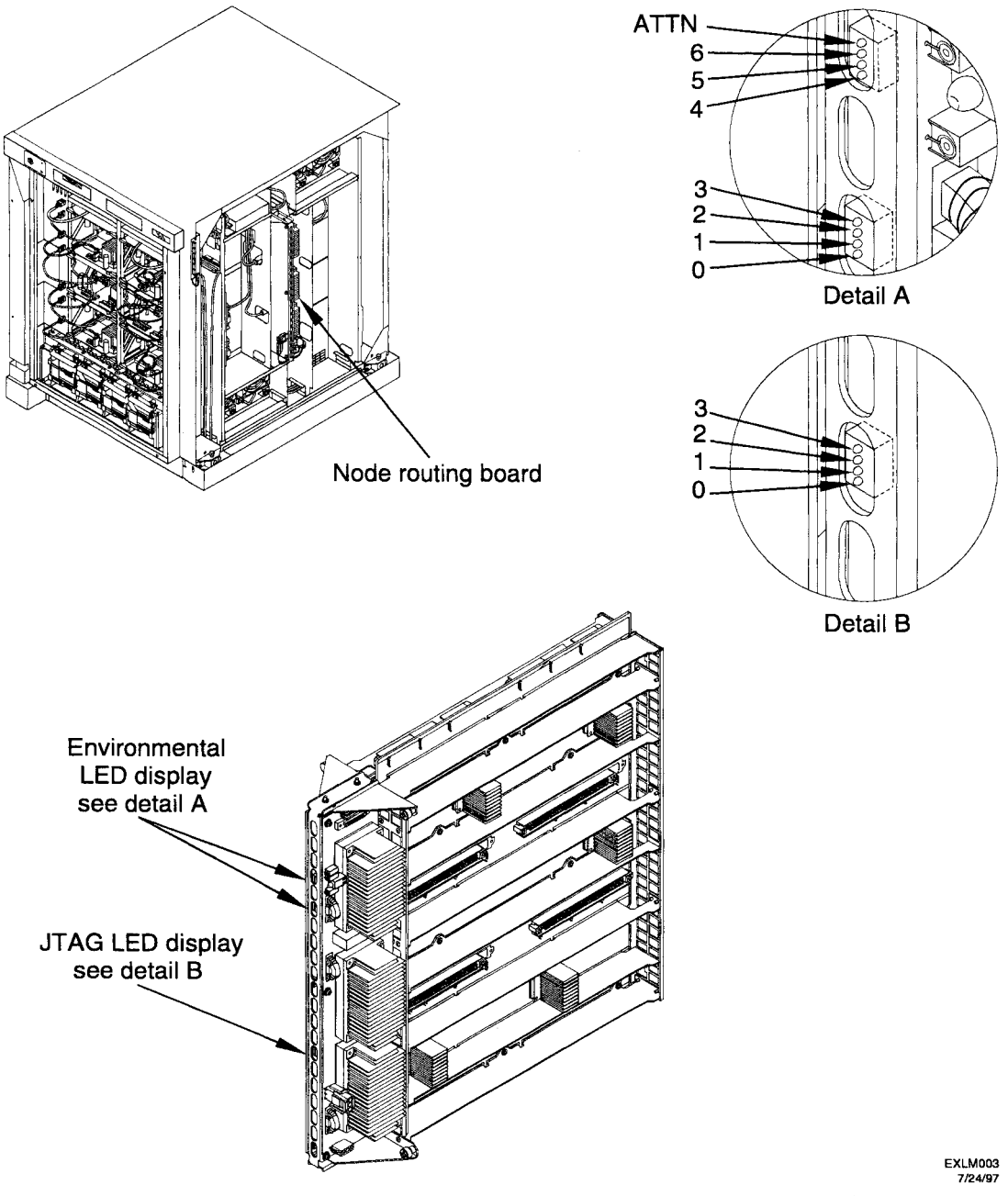


Figure 13 Core utilities board (ECUB) LEDs



Troubleshooting at initialization

To determine the board fault is often a process of elimination:

- Take a system to minimum configuration (as shown in Table 2 on page 12
- Repeat the sequence of events that lead to the error by running the memory boards one pair at a time, or one processor at a time

Table 9 is a troubleshooting guide for the server hardware during initialization. The table summarizes the sequence of events from engaging the breakers to operating system start-up, showing symptoms of possible error states and the recommended action for recovery. See the sections that follow for more information and examples.

Table 9 Initialization errors

Phase	Symptom	Action
System OFF	Green indicator next to circuit breaker not on	• Check customer branch service breaker • Verify possible bad indicator by measuring voltage at test points (See
Engage breaker	Power supply fans did not spool up	• Check power supply switch. • Check power supply circuit breaker • Replace respective supply, if Push to Reset breaker is indicating, then reset

Table 9 Initialization errors —**(continued)**

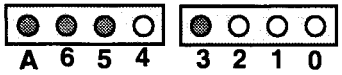
Phase	Symptom	Action
Keylock ON or ENABLE	System boards not powering up. (no "DC ON" light)	• Check for 48V failure, if fans are not OK • Check and replace the core utilities board (ECUB) power converter power, if fans are OK
	System boards not powering up. ("DC ON" light blinks)	• Check ECUB LEDs for environment errors, probably a "YO-YO" error or insufficent supplies • Verify redundency switch and supplies are seated and turned on
	System boards not powering up. ("DC ON" solid)	• Check ECUB LEDs for environmental errors, probably power failure reported from a board • Verify all 48V cables are plugged in and if so replace offending board
Database generation errors	`ccmd` fails to read the cop chip on a board properly	See Chapter 7,"Database generation errors"
	Broken scan ring	• Verify with `est` • See Chapter 7, "Database generation errors"
Core utilities board (ECUB)	ECUB LED error shows  i.e., HEX CODE = 68	• Match hex code from LEDs to tables in Chapter 10, "ENRB Troubleshooting" • Run `pce_util` • Check teststation window for an error

Table 9 Initialization errors —**(continued)**

Phase	Symptom	Action
POST	Processor did not report in	• Verify with `est` • See Chapter 12, "Processor errors"
	Memory fails to initialize because memory is not visible	• Verify with `dcm` to determine which memory is failing • See Chapter 10, "ENRB Troubleshooting"
	Processor or memory causes a timeout or hang	• Check for bad memory or CPU board (See Chapter 8, "POST errors") • Take node to minimum configuration as shown in Table 2 on page 12
	CPU traps: after POST as OBP begins to boot, OBP hangs	• Check board server hangs on • Check the LCD • See Chapter 8,"POST errors"
	HPMC (High Priority Machine Check)	See Chapter 13, "Errors and events"
	Time-out or hang during initialization	See Chapter 13, "Errors and events"
OBP	Hard errors	See Chapter 13, "Errors and events"
	Advisory error	See Chapter 13, "Errors and events"
SPP-UX - OS	Soft errors	See Chapter 13, "Errors and events"

Database generation errors 7

Overview

This chapter discusses failures between the time that the key switch is turned on and the database generation completes its process. The teststation allows the user to configure the node. The teststation daemon, `ccmd`, is responsible for monitoring the node and reporting back configuration information, error information, and general status. For more information on configuration management, consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

ccmd utility

Two utilities, ccmu and xconfig, are each capable of reading or writing configuration information and changing it. The OpenBoot Program can also be used to modify the configuration. See Chapter 9, "Open boot program."

The teststation is required in system power-up, monitoring, testing, and error logging. It is not required for normal operation of a node.

The main tool to initiate communications is the Complex Configuration Management Daemon (ccmd).

```
ccmd [-d]
```

Very few of the diagnostic utilities can run without the information database created by ccmd.

If no nodes are responding, ccmd clears all node data and waits for a node to respond. If a node powers up, the entire database is rebuilt.

If a node has stopped responding, ccmd clears just that node's data in the database.

If ccmd detects a hard error, it starts the hard_logger script to extract additional information from the node through the JTAG interface.

ccmd sends output to the console. If running under X-windows as sppuser, it sends its output to the sppuser window. The -d debug option generates a substantial amount of console output.

ccmu utility

The Convex Configuration Management Utility (ccmu) is used to view and modify a limited set of parameters from the sppuser shell.

ccmu is a text-based tool that can modify the reconfiguration parameters initialized by POST.

ccmu is started by the user from the teststation either in command line or interactive mode. Once started, it attaches to the teststation database created by ccmd.

ccmu also reads the /spp/data/complex.info file to maintain a list of all possible nodes that could be reconfigured.

Note

Crosscheck the teststation database and the complex.info file with the `system -check` command.

ccmu command line parameters have the following format:

```
ccmu command [[: command].... [: command]]
```

Each command is the same format as those of the interactive ccmu.

In the interactive mode, ccmu is started by the command, ccmu, executed at a shell prompt. The following user prompt appears when ccmu is running interactively:

```
ccmu>
```

When a command is issued, ccmu communicates with the system through the JTAG interface to read or write the data and instructions required to accomplish the command.

For more information on ccmu, consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

Example of updating COP chips on boards

COP chips (serial EEPROMs) are located on the major boards with information such as serial number, assembly revision, wire revision, truncated board number, and so on. This utility can be used to update this information (copmod) on the ENRB.

```
sppuser> ccmu
ccmu > copmod 0 enrb
```

Enter the appropriate information as prompted by ccmu.

```
ccmu > cop 0 /verify all COP information is correct /
ccmu > quit
```

The node must be powered down and powered back on, or use the kill command on the ccmd process.

For more information on ccmd, consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

ccmd related errors

After powering up a system and allowing it to initialize, allow the database generation to complete and check the teststation console output as shown in the example below:

```
INFO: node id 0 was found
WARNING: board pb21 is not properly copped
Bad board id is -2147479536
INFO: Database generation is complete
```

If the symptoms shows that the board does not have the correct information (in the COP chip) it has not been (updated) copped:

Step 1 Type `ccmu` in the sppuser window.

Step 2 Type `copmod 0` *board* (where *board* is the board in the warning message).

Step 3 Enter the board information: four digit part number, serial number, assembly revision, and wire revision.

Step 4 Verify the information was correctly entered by typing `cop 0`, and then type `quit`.

Step 5 If the COP information does not verify correctly, then the COP circuit is bad, and the board should be replaced.
If the COP information does verify, then this may indicate the COP circuit fails intermittently, or the board was not copped correctly.

`xconfig` utility

`xconfig` is the graphical tool that can modify the parameters initialized by POST to reconfigure a node. Use it to also see the configuration state.

The names, within the utility, are consistent with the hardware names, since individual configuration parameters are hidden to the user. The drawback of `xconfig` is that it cannot be used as a part of script-based tests, nor can it be used for remote debug.

`xconfig` is started from a shell as `ccmu` is. It reads the teststation database and the possible nodes from `/spp/data/complex.info`

Information on a node is read and interpreted to form the X-windows display shown in the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

Broken scan ring

If a board is broken, an error appears as shown below.

```
INFO: node id 0 was found
WARNING: board pb21 is not properly copped
```

Lists of bad JTAG IDs and ring numbers are displayed.

```
Bad board id is -2147479536
INFO: Database generation complete
```

Use `est` to troubleshoot a broken scan ring.

Step 1 Power up the system.

Step 2 Allow the system to initialize (database generation is complete).

Step 3 Check the COP information (board ID in this case) because it must be correct for `est` to work.

Step 4 To correct the COP information before running `est` type:

```
sppuser> ccmu
ccmu > copmod 0 pb21
```

Enter the appropriate information as prompted by `ccmu`.

Step 5 Verify the COP information entered is correct by typing:

```
ccmu > cop 0 /verify all COP information is correct /
ccmu > quit
```

If the board is broken, an error will show up as in the above example

Step 6 In the teststation console, type the following to load `est`.

```
cd /spp/est
est 0
```

```
Excalibur Scan Test 001.000.001.000 1997/01/22 11:20:116 Steven Terry
.....................................
.........
```

Step 7 When the main menu comes up, choose one of these options:

```
r ...board level scan tests (return)
d ...board level dc tests (return)
a ...board level ac tests (return)
```

If a test passes, `PASSED` or `0 ERRORS` will display.

If the test fails, information is supplied showing source part location, destination part location, and pin numbers. Expected and actual bit values, signal names, and, in some cases pattern numbers are also shown. The examples below show two errors that can result from running `est`.

An example of `est` failing on an SRAM on a processor board (EPB) is shown:

```
DC Connectivity...
   SRAM64|pb21(6) Z055N9|42|actual: 0|expected:1
     wire: DATA041
      SRAM64|pb21(6) Z055N9|DQA6|6L
      UCHIP|pb21(6) U039P7|DCD041|AA31
```

An example of `est` failing the pcxu to a processor agent chip (EPAC) on the node routing board (ENRB) is shown:

```
DC Connectivity...
   UCHIP|pb21(6) U039P7|536|actual:0|expected:1
     wire: R04DAT7
      EPAC|enrb(1) U022E3|R00_DAT[7]|G26
      UCHIP|pb21(6) U039P7|ADDRDATA7|C27
```

POST errors

8

Overview

This chapter discusses failures between the time that the key switch is turned on and Open Boot Program (OBP) starts its boot process. See Chapter 9 for more information on OBP.

The processor utilities chip (EPUC) provides the core utilities board (ECUB) a means to apply interrupts and error messages to the processors and to receive control messages from the processors. The processor utilities chip (EPUC) contains firmware in the EEPROM known as Power On Self Test (POST) routine.

Upon powerup, all processors and hardware must be initialized before the node proceeds with booting. POST begins executing and brings up the node from an indeterminate state and then executes the Open Boot Program (OBP).

None of the POST routines can be directly controlled via a user interface. Program control is provided by a set of configuration parameters (processing flags and variable definitions) stored in EEPROM by OBP, `ccmu`, or `xconfig`.

The error reporting modules display error codes for all fatal errors that occur during the POST execution. Any errors that reconfiguring the hardware can correct are reported to OBP. POST status is reflected on the LCD display.

POST performs the following tasks:

- Initializes each processor in the node
- Validates all shared data structures within the EEPROM
- Initializes the core logic required to start OBP execution
- Determines node configuration
- Initializes all ASICs
- Initializes main memory
- Sets up CTI cache
- Invokes OBP

POST passes node configuration and any options to OBP via shared data structures.

POST modules

POST contains the following modules:

- Core Logic SRAM Initialization—Initializes all the SRAM space in the core logic to a known state. It also initializes parity for the SRAM.
- Configuration Determination and ASIC Hardware Initialization—Determines the ASIC population and sets the ASIC CSRs to a default state to prepare for main memory initialization. It initializes core logic utilities ASICs at the beginning of this process.
- Main Memory Initialization—Configures the memory interleave hardware and initializes all of main memory to valid data, ECC, and tag values for both local memory and CTI cache. The main memory population is reported to OBP.
- Error Reporting—Sets up and maintains the boot error log and boot status word in the EEPROM and reports errors to the LCD.

Example of sppconsole window output

The following is an example of correct output to the sppconsole window during POST initialization and OBP boot.

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
Probing CPUs.
Completing core SRAM initialization.
Initializing main memory.
   Probing memory: MB0L, MB1L, MB2R, MB3R, MB4L, MB5L, MB6R, MB7R
   Initializing MB0L........
   Initializing MB1L........
   Initializing MB2R........
   Initializing MB3R........
   Initializing MB4L........
   Initializing MB5L........
   Initializing MB6R........
   Initializing MB7R........
Booting OBP.
OPB Power-On Boot on [0:0]
SPP2000, OBP Release 3.0.2, compiled 97/01/07 11:55:13
16 CPUs, 4096 MB memory installed, 3 PCI units available.
Complex Serial Number: -1, Node Serial Number 2011255.
Network address 0:a0:d9:0:b0:77, OBP IP Number 15.99.111.150.
Using sppux boot-mode
[0:0] ok
```

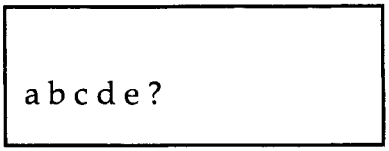
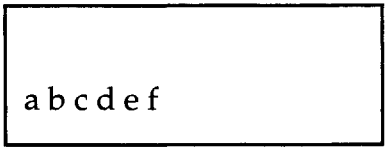
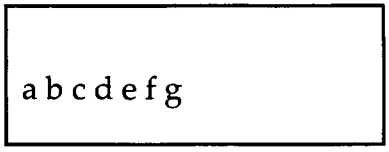
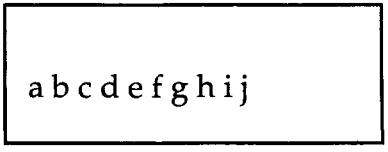
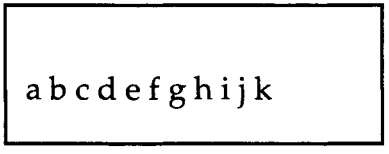
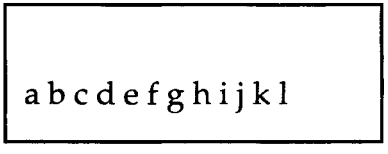
Power On Self Test (POST)

These are the POST steps the LCD shows as a node is powered-on.

Table 10 POST steps

LCD display	Description	LCD
POST Initializes	Power-On Self Test starts with LCD power up	IIII MIII IIII IIII POST Rev 0.10.0.0 Monarch: PB2L
a	Monarch CPU selected	a
b	POST code checksum	a b
c	Test controller code checksum	a b c
d	OBP code checksum	a b c d
e	Configuration parameter checksum	a b c d e

Table 10 POST steps —**(continued)**

LCD display	Description	LCD
?	Rebuilding configuration (due to checksum failure or data corruption)	
f	Starting core logic hardware	
g	EPUC/EMUC CSR initialization	
h -> j	ECUB test - core logic SRAM	
k	Zero filling core logic SRAM	
l	Starting C-runtime environment	

Processor - POST failure

If a board shows up in the teststation console as not reporting in or hangs during initialization, like the example below, see Chapter 12, "Processor errors."

```
SPP2000, POST version 1.10.0.0, compiled 1997/01/13 14:38:03
Monarch: PB3L
Probing CPUs
**** WARNING **** PB3L is installed but did not report in
```

Memory - POST failure

If all installed memory is not visible during initialization, as in the example below, go to the section on memory failures and use `dcm` to verify which memory board, bank, and DIMMs are failing.

```
Initializing main memory
Probing memory: MB0L, MB1L
**** WARNING **** Some or all of main memory was hardware deconfigured
Initializing MB0L ....-------- (indicates the board at fault)
Initializing MB1L .... #### (indicates the board was deconfigured)
```

OBP hangs and CPU traps

OBP hangs or CPU traps occur after the system has begun to boot OBP. In the example below, the `Booting OPB` sequence appears to complete but hangs at the `Booting OBP` step.

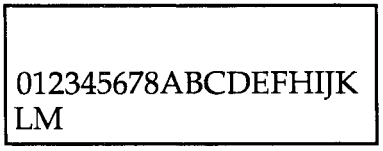
This failure can be caused by a processor or memory board. See Chapter 12, "Processor errors" or Chapter 11, "Memory board errors."

```
SPP2000, POST version 1.10.0.0, compiled 1997/01/13 14:38:03
Monarch: PB2L
Probing CPUs
Initializing main memory.
  Probing memory: MB0L,MB1L
  Initializing MB0L.........
  Initializing MB1L.........
Booting OBP. (OBP hangs at this point)
```

Also the LCD panel on the front left side of the server shows either one of these displays. The startup is hung at this point without finishing the sequence.

Figure 14 CPU hang at 2 and 3

Figure 15 CPU hangs at L and M



Check the teststation console for any hard errors.

Memory initialization timeout

The memory initialization can timeout, or hang. This can be caused by the system hanging on a particular board or a hard error. Below is a normal memory initialization.

```
SPP2000, POST version 1.10.0.0, compiled 1997/01/13 14:38:03
Monarch: PB2L
Probing CPUs
Initializing main memory.
  Probing memory: MB0L,MB1L
  Initializing MB0L.........
  Initializing MB1L.........
Booting OBP.
```

Compare the example above with a memory hang example below:

```
SPP2000, POST version 1.10.0.0, compiled 1997/01/13 14:38:03
Monarch: PB2L
Probing CPUs
Initializing main memory.
  Probing memory: MB0L,MB1L
  Initializing MB0L.........
Initializing MB1L.. (at this point POST hung after 2 dots)
```

The error can show up in the LCD panel on the front left side of the node, or a hard error can result from the error not a board fault. A hard error will show up in the teststation console. This is usually caused by a bad memory board or DIMM.

See Chapter 11, "Memory board errors."

Other POST errors

If you see the following errors during start-up, follow the actions to correct the problems.

Table 11 POST errors

Error	Corrective actions
`**** WARNING **** Rebuilding POST boot configuration map`	• Check settings using printenv • Check if boot-mode = sppux • Use the following, if using core boot-mode: `setenv boot-mode sppux [normal]` or `setenv boot-mode hpux` (for booting HP-UX) • Enter `do_reset` in the sppuser window
`**** WARNING **** Some or all of Main Memory was hardware deconfigured`	Use `dcm 0` to check the memory error. See the example in Chapter 11, "Memory board errors"
`**** WARNING *** PB4L is installed but did not report in`	• Check for bad solder connection at the runway bus clock sockets • Check clock at feed through on the opposite side of the node routing board (ENRB) • Check if the CPU in the message is plugged in • Check for a bad processor agent chip (EPAC) or gate array socket; verify this with `est` diagnostic
`****WARNING *** PB1L is idle but timed out during ping operation`	Check to see if the runaway bus delay line is plugged all the way in its socket on the node routing board (ENRB)

For more information on POST consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

Open Boot Program (OBP)

9

OBP overview

This chapter introduces common Open Boot Program (OBP) commands, parameters, and the OBP process. Troubleshooting OBP errors is also covered.

- OPB commands
- OPB parameters
- OBP boot process
- OBP booted
- OPB errors

OBP commands

The most common OBP commands used in troubleshooting are listed in Table 12 .

Table 12 Common OBP commands

Command	Description
`.attributes`	Displays information about a specific device controller
`cd`	Changes hardware paths (directories) within OBP
`devalias`	Displays the nvaliases
`execute-device -method`	Executes a device method, commonly used with the `show-children` option
`fwcp`	Copies firmware from the teststation disk to flash ram on the core utilities board (ECUB)
`lifls`	Displays information on a `lif` file system (i.e. contents of flash)
`list`	Reads the directory contents of any disk drive
`ls`	Lists the devices under the current branch of the hardware tree
`mkmap`	Maps a logical device number to a hardware device
`nvalias`	Builds aliases for hardware paths
`nvunalias`	Erases nvaliases
`printenv`	Displays the entire set of user definable parameters or display a single parameter by using arguments
`pwd`	Displays the current hardware path, inside OBP
`reset`	Restarts POST after changes are made to parameters
`rmmap`	Removes entries in NVRAM made with the mkmap command
`setenv`	Sets parameter values (i.e., `setenv boot-module` sets the mode of operation for POST to boot up in)
`set-default`	Sets parameter values back to the factory default. Use an argument to prevent all OBP parameters from being reset to default.
`show-children`	Displays information about all devices attached to the specified controller
`show-part`	Displays partition information for a disk drive given in the same format as `diskutil`
`show-devs`	Display the hardware devices that OBP knows about
`source`	Runs scripts, usually located in the teststation directory

Use the `man` pages for command line options.

OBP parameters

The common parameters used in Booting OBP are summarized below in Table 13 .

Table 13 Common OBP parameters

Parameter	Description	Example(s)
`boot-module`	Sets environment module to boot after POST completes	`setenv boot-module idle`
		`setenv boot-module obp`
		`setenv boot-module diags`
`boot-mode`	Sets the operating system to boot to `core` - main memory (not used and allows for parameter debugging and maintenance)	`setenv boot-mode core`
	`sppux` - normal SPP-UX	`setenv boot-mode sppux`
	`hpux` - for booting HP-UX	`setenv boot-mode hpux`
`pci[#]-fcode-enable`	Sets an EPIC/Slot basis to enable a disk drive to be bootable	
`boot-device`	Sets default root drive located internally next to the core utilities board (ECUB)	`/pci@fe,1000/qlisp@1000,0/sd@2,0:a`
`boot-directory`	Sets default as `/stand/spp3` defined by boot-device parameter	Files found in the root directory include mach, server and tuneables
`boot-file`	Sets default as mach in `/stand/spp`	
`boot-args`	Sets argument used with the boot command to identify a different root directory to be mounted	
`load-tuneables`	Enables or disables loading of the OS tunables	
`auto-boot?`	Sets paramater to true to enable automatic booting of the OS from the keyswitch	

OBP boot process

Table 14 illustrates the normal OBP process shown on the LCD displays.

Table 14 OBP process

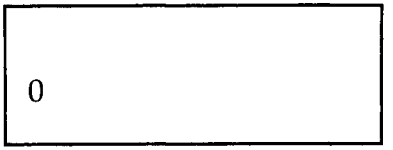
LCD display	Indicator description	LCD
0 ->	Monarch selected CPU init LCD init	
0 -> 1	Initial bootstrap-trap	
1 -> 2	OBP relocation Copy test and data from ROM to RAM	
2 -> 3	Re-idle slaves Monarch enters Forth interpreter	
3 -> 4	Initialize Forth heaps	
4 -> 5	Initialize High Priority Machine Check (HPMC) guard handler for later I/O probing	

Table 14 OBP process —**(continued)**

LCD display	Indicator description	LCD
6 -> 7	Imitate UART device driver	01234567
7 -> 8	Initialize the /core package Initialize sonic DMA 'heap' memory manager	012345678
8 -> A	Initialize Runtime Trap handler	012345678A
A -> B	Initialize machine-code debugger	012345678AB
B -> C	Initialize HPMC/TOC trap	012345678ABC
C -> D	Initialize Forth dictionary limits	012345678ABCD

Table 14 OBP process —**(continued)**

LCD display	Indicator description	LCD
D -> E	Initialize Virtual Memory	012345678ABCDE
E -> F	Probe /memory device	012345678ABCDEF
F -> G	Initialize alarm clock trap Currently disabled	012345678ABCDEFG
G -> H	Check NVRAM checksum Optional rebuild	012345678ABCDEFH
H -> I	Set 'stand-alone?' state variable to true	012345678ABCDEFHI
I -> J	Select full or restricted command mode Security	012345678ABCDEFHIJ

Table 14 OBP process —(continued)

LCD display	Indicator description	LCD
J -> K	Initialize FCode package compiler	012345678ABCDEFHIJK
L -> M	Probe CPUs Perform self calibration	012345678ABCDEFHIJK LM
M -> N	Initialize tty modes Currently disabled	012345678ABCDEFHIJK LMN
N -> O	Create banner strings	012345678ABCDEFHIJK LMNO
P -> Q	Probe PCI I/O system hierarchy	012345678ABCDEFHIJK LMNOPQ

OBP booted

Once OBP is booted, the operating system (SPP-UX) is booted.

Table 15 OBP booted

Phase	Process description	LCD display of codes
OBP	OBP Booted F - Forth	0 (0,0) SN 20ffffff 1111 F111 --11 ----
SPP-UX booted	SPP-UX is booted and system is being used and active	00 (0,0) CSN -000001 KIUU<ISUU< - - FU<UUUU HP-Exemplar S-Class Convex SPP-UX
	Description	Letter
	Kernel	K
	Idle	I
	Forth	F
	Server	S
	User	U
	Monarch processor - first initialized	M
	Installed processor but not responding during POST	D
	User disabled	d

OBP errors

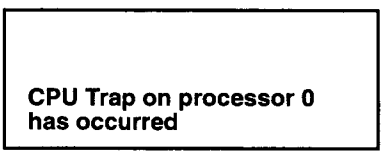
OBP errors occur during initialization and can show up as hard errors because POST passes and the server appears to hang while booting the OBP module.

In most cases the following occurs:

1. The output from powerup in the sppconsole window looks like the following example:

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
Initializing main memory.
  Probing memory: MB2R, MB3R, MB4L, MB5L
  Initializing MB2R ........
  Initializing MB3R ........
  Initializing MB4L ........
  Initializing MB5L ........
Booting OBP.
OPB Power-On Boot on [0:0]
```

2. The front panel LCD indicates that a CPU trap on processor # has occurred (where # stand for the processor number that failed).



3. After a few seconds, the attention LEDs flash.
4. Shortly after this information, the output from the hard_logger (information gathered about the hard error) scrolls in the sppconsole message window as shown in the example below:

```
*** questioning suspect: erac[1]
** Erac 1 needs to be interrogated:
         its hard error group pin indicates
         that only this chip was the first to encounter this error
================================================================================
erac_interrogator is running on NODE n0 ERAC r11

error_cause          = 0x3e
error_info           = 0x665a
error_config         = 0x1db
error_group          = 0x0
--------------------------------------------------------------------------------
hard error Group bit = 0x0 The ERAC's hard error pin WAS NOT driven
                           by another chip.
error_info phase     = 0xd
error_info S         = 0x0
--------------------------------------------------------------------------------
```

```
error_cause register indicates 5 error (s):
bit   severity   error name
---   --------   ----------
 0    advisory   Latch Array Read Parity Error
 1      hard     Input Queue Overflow
 2      hard     Input Parity Error on Critical Cycle
 3    advisory   Input Parity Error on Non-Critical Cycle
 4      hard     Null Route Mask
*EX!*    Running extractor r_queue_over_error n0:21:internal:r11 m2:
Event Code = 0xf00
-------------------------------------------------------------------------
NODE 0 ERAC R1L PORT M2 detected a Input Queue Overflow Error
     r_la_hold                    = 0
     c_queue_over                 = 1* error was detected
     Scan Fields
-------------------------------------------------------------------------
     core.r_err_cause [0:6]       = 3e
     core.r_err_info [1:15]       = 6642
     la0.r_di[0:31]               = ec0a4a00
     la0.r_wr_ad[0:5]             = 3d
     la0.r_we                     = 0

     ERAC Port                    = EMAC 2
     Packet Source                = EMAC MB5L
```

5. The output calls out the error in the `Packet Source` section of the file as a problem with the routing attachment chip (ERAC) detecting an error from data sent from the memory access chip (EMAC) on the memory board MB5L.

Run `est` to verify the scan ring passes.

Node routing board (ENRB) troubleshooting

10

Overview

The chapter covers troubleshooting the node routing board (ENRB) using the groups of core utilities board (ECUB) LEDs and other utilities for the S-Class and X-Class Servers.

- Environmental LEDs
- JTAG status LEDs

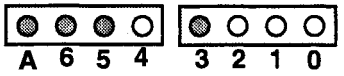
Environmental errors are monitored and reported by the core utilities board (ECUB). They can occur on powerup or at any time after the node has been powered up and running. When an environmental error occurs, the LEDs on the front of the node (Attention light bar LEDs) flash, and the error code displays on the core utilities board (ECUB) environmental LEDs.

Core utilities board (ECUB) LEDs

The LEDs located on the core utilities board (ECUB) are visible from the front of the node, after removal of the front skin and EMI panel. See Figure 13 on page 50 for LED location. There are two sets of LEDs:

The upper set displays environmental errors, along with other system interrupts, such as a hard error. (See Table 16 through Table 24 for LED explanations) (See Chapter 6,"System initialization faults" for the location)

Figure 16 Environmental LEDs on ECUB



Hex code = 68

Lower LEDs indicate the JTAG status, which includes the 68360 processor and scan bus. (See Table 27 for explanation of the LEDs.)

The Attention LEDs, on the front of the server, flash when an error is present. On the teststation, `man leds` is available to decode these environmental codes. Also the power utility `pce_util` can be used to display environmental codes when the skin is not removed but only after database generation is complete.

Power on detected errors

This section covers core utilities board (ECUB) LED errors from highest to lowest priority detected at power on. The Attention LED on the core utilities board (ECUB) turns on, and the Attention light bar on the front of the node flashes to indicate the presence of an error code listed below. Additionally, only the highest priority error is displayed. Once remedied, an error that is cleared may expose a lesser priority error. Errors are listed in sequence from the highest to lowest priority.

Replacement and removal procedures (used in the corrective actions below) are given in "Component removal and replacement" chapter.

Note

Errors from LED hex-code 00 through hex code 67 shut the system down and errors from hex-code 68 through 73 leave the system up.

Table 16 ECUB detects power on error

LED	Fault	Symptoms	Corrective action
00	3.3V error (highest priority)	1. 5V is up 3.3V is not. 2. Teststation interface will not function.	• Replace the 3.3V fuse, if the ECUB has recently been probed or cabled. • Replace the ECUB fuse; see Appendix A
01	ASIC Install 0 (ENRB)	1. Incorrect rotation or part in one of the processor agent chip (EPAC) sockets. 2. Incorrect rotation or part in one of the routing (XBAR) attachment chip (ERAC) sockets.	• Inspect all EPAC (8) and ERAC (4) installations in the node since last power up and correct. • Replace ENRB.
02	ASIC Install 1 (EMB)	1. Incorrect rotation or part in one of the memory access chip (EMAC) sockets. 2. Incorrect rotation or part in one of the toroidal access chip (ETAC) on memory board (EMB).	• Replace any memory board (EMB) installed since last power up. • Rotate known good EMB through slots.
03	FPGA not OK	Core utilities board (ECUB) monitoring utilities chip (EMUC) cannot get correct program transfer from EEPROM on power up.	• Cycle the node power using the Key switch. • Replace ECUB.

Table 16 ECUB detects power on error —**(continued)**

LED	Fault	Symptoms	Corrective action
04	DC OK error (Upper Left)	1. Power supply reporting failure (DC OK) prior to core utilities board (ECUB) after keylock turn on, but prior to ECUB power on sequence. 2. If the node is equipped with redundant power supplies and the ECUB "redundancy switch" (Figure 87) is down this is the first of two or more supplies reporting failure. 3. With supplies and ECUB switch in the nonredundant configuration (switch=up) this is the first of one or more supplies reporting failure.	• Verify the yellow (dc) and green (ac) LEDs on all installed 48V supplies, leaving keylock on. • Replace upper left supply, if yellow (dc) LED and no green (ac) LED. • Check, if no yellow LED : – Power supply switch is on. – Power supply properly seated. – Power supply circuit breaker is OK. • Replace the upper left supply, if circuit breaker is open or no yellow (dc) LED after the check.
05	DC OK error (Upper Right)	1. Power supply reporting failure (DC OK) prior to core utilities board (ECUB) after keylock turn on, but prior to ECUB power on sequence. 2. If the node is equipped with redundant power supplies and the ECUB "redundancy switch" (Figure 87) is down this is the first of two or more supplies reporting failure. 3. With supplies and ECUB switch in the nonredundant configuration (switch=up) this is the first of one or more supplies reporting failure.	• Verify the yellow (dc) and green (ac) LEDs on all installed 48V supplies, leaving keylock on. • Replace upper right supply, if yellow (dc) LED and no green (ac) LED • Check, if no yellow LED: – Power supply switch is on. – Power supply properly seated. – Power supply circuit breaker is OK. • Replace the upper right supply, if circuit breaker is open or no yellow (dc) LED after the check.

Table 16 ECUB detects power on error —**(continued)**

LED	Fault	Symptoms	Corrective action
06	DC OK error (Lower Left)	1. Power supply reporting failure (DC OK) prior to core utilities board (ECUB) after keylock turn on, but prior to ECUB power on sequence. 2. If the node is equipped with redundant power supplies and the ECUB "redundancy switch" (Figure 87) is down this is the first of two or more supplies reporting failure. 3. With supplies and ECUB switch in the nonredundant configuration (switch=up) this is the first of one or more supplies reporting failure.	• Verify the yellow (dc) and green (ac) LEDs on all installed 48V supplies, leaving keylock on. • Replace lower left supply, if yellow (dc) LED and no green (ac) LED. • Check, if no yellow LED: – Power supply switch is on. – Power supply properly seated. – Power supply circuit breaker is OK. • Replace the lower left supply, if circuit breaker is open or no yellow (dc) LED after the check.
07	DC OK error (Lower Right)	1. Power supply reporting failure (DC OK) prior to core utilities board (ECUB) after keylock turn on, but prior to ECUB power on sequence. 2. If the node is equipped with redundant power supplies and the ECUB "redundancy switch" (Figure 87) is down this is the first of two or more supplies reporting failure. 3. With supplies and ECUB switch in the nonredundant configuration (switch=up) this is the first of one or more supplies reporting failure.	• Verify the yellow (dc) and green (ac) LEDs on all installed 48V supplies, leaving keylock on. • Replace lower right supply, if yellow (dc) LED and no green (ac) LED. • Check, if no yellow LED: – Power supply switch is on. – Power supply properly seated. – Power supply circuit breaker is OK. • Replace the lower right supply, if circuit breaker is open or no yellow (dc) LED after the check.

Table 16 ECUB detects power on error —**(continued)**

LED	Fault	Symptoms	Corrective action
08-11	48V error NPSUL failure PWRUP=0-9	1. Error occurs when 48 volt distribution falls below 42 volts during powerup state displayed. Powerup state indicates which loads are being turned on. Refer to Tables 2. Excessive load on 48 volts due to an inadequate number of functioning 48 volt supplies or overload condition on 48V bus. 3. Possible node power supply (NPS) upper left failure.	• Check NPSUL (upper left) seating. • Replace NPSUL (upper left) power supply. • Look at boards being powered during state displayed for possible overload, if error persists.
12-1B	48V error NPSUR failure PWRUP=0-9	1. Error occurs when 48 volt distribution falls below 42 volts during powerup state displayed. Powerup state indicates which loads are being turned on. Refer to Tables 2. Excessive load on 48 volts due to an inadequate number of functioning 48 volt supplies or overload condition on 48V bus. 3. Possible node power supply (NPS) upper right failure.	• Check NPSUL (upper right) seating. • Replace NPSUL (upper right) power supply. • Look at boards being powered during state displayed for possible overload, if error persists.
1C-25	48V error NPSLL failure PWRUP=0-9	1. Error occurs when 48 volt distribution falls below 42 volts during powerup state displayed. Powerup state indicates which loads are being turned on. Refer to Tables 2. Excessive load on 48 volts due to an inadequate number of functioning 48 volt supplies or overload condition on 48V bus. 3. Possible node power supply (NPS) lower left failure.	• Check NPSUL (lower left) seating. • Replace NPSUL (lower left) power supply. • Look at boards being powered during state displayed for possible overload, if error persists.

Table 16 ECUB detects power on error —**(continued)**

LED	Fault	Symptoms	Corrective action
26-2F	48V error NPSLR failure PWRUP=0-9	1. Error occurs when 48 volt distribution falls below 42 volts during powerup state displayed. Powerup state indicates which loads are being turned on. Refer to Tables 2. Excessive load on 48 volts due to an inadequate number of functioning 48 volt supplies or overload condition on 48V bus. 3. Possible node power supply (NPS) lower right failure.	• Check NPSUL (lower right) seating. • Replace NPSUL (lower right) power supply. • Look at boards being powered during state displayed for possible overload, if error persists.
30-39	48V error (maintenance) no supply failure reported PWRUP=0-9	1. Error occurs when 48 volt distribution falls below 42 volts during powerup state displayed. Powerup state indicates which loads are being turned on. Refer to Tables 2. Excessive load on 48 volts due to an inadequate number of functioning 48 volt supplies or overload condition on 48V bus. 3. Possible node power supply (NPS) failure.	• Check for adequate power supply configuration, if the node has recently been reconfigured. • Rotate spare supply through all locations to isolate. (Possible supply failure without indication.)
3A	48V Yo Yo error	1. Core utilities board (ECUB) lost and then regained 48V power without the machine being turned off or ac power failure. 2. Core utilities board (ECUB) will display this error and not power on the system.	• Locate and correct intermittent 48V failure. • Verify power supplies are Revision C or higher. • Keylock power cycle the node to clear the Yo Yo bit, if problem is resolved.

Table 16 ECUB detects power on error —**(continued)**

LED	Fault	Symptoms	Corrective action
3B	ENRB power fail (ENRBPB)	1. VDD (3.3V) error on node routing board power board (ENRBPB). 2. Midplane power fails and entire node will power down. 3. Core utilities board (ECUB) still active.	• Replace ENRBPB (supply) or ENRB (load). • Keylock power cycle the node to clear the error, if problem is resolved.
3C	Clock fail	1. Core utilities board (ECUB) monitors clock on node routing board (ENRB).	• Replace node routing board (ENRB). • Replace core utilities board (ECUB).

EMUC detected errors

This section covers errors detected by the monitoring utilities chip (EMUC) on the core utilities board after power-on. See Figure 31 on page 153 for memory and processor board locations.

Table 17 ECUB detects memory power fail

LED	Fault	Symptoms	Corrective action
40	MB0L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 0 left (MB0L). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB0L. • Replace MB0L.
41	MB1L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 1 left (MB1L). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB1L. • Replace MB1L.
42	MB2R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 2 right (MB2R). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB2R. • Replace MB2R.
43	MB3R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 3 right (MB3R). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB3R. • Replace MB3R.

Table 17 ECUB detects memory power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
44	MB4L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 4 left (MB4L). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB4L. • Replace MB4L.
45	MB5L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 5 left (MB5L). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB5L. • Replace MB5L.
46	MB6R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 6 right (MB6R). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB6R. • Replace MB6R.
47	MB7R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on memory board 7 right (MB7R). 3. Core utilities board (ECUB) powers down the system.	• Replace memory power board (EMPB) of MB7R. • Replace MB7R.

Table 18 ECUB detects processor power fail

LED	Fault	Symptoms	Corrective action
48	PB0L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 0 left (PB0L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB0L. • Replace PB0L.
49	PB1L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 1 left (PB1L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB1L. • Replace PB1L.
4A	PB2R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 2 right (PB2R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB2R. • Replace PB2R.
4B	PB3R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 3 right (PB3R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB3R. • Replace PB3R.
4C	PB4L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 4 left (PB4L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB4L. • Replace PB4L.

Table 18 ECUB detects processor power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
4D	PB5R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 5 right (PB5R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB5R. • Replace PB5R.
4E	PB6L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 6 left (PB6L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB6L. • Replace PB6L.
4F	PB7R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 7 right (PB7R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB7R. • Replace PB7R.
50	PB0R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 0 right (PB0R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB0R. • Replace PB0R.
51	PB1L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 1 left (PB1L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB1L. • Replace PB1L.

Table 18 ECUB detects processor power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
52	PB2R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 2 right (PB2R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB2R. • Replace PB2R.
53	PB3L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 3 left (PB3L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB3L. • Replace PB3L.
54	PB4R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 4 right (PB4R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB4R. • Replace PB4R.
55	PB5L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 5 left (PB5L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB5L. • Replace PB5L.

Table 18 ECUB detects processor power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
56	PB6R Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 6 right (PB6R). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB6R. • Replace PB6R.
57	PB7L Power Fail	1. 3.3V dropped below acceptable level. 2. Core utilities board (ECUB) detected a power loss on processor board 7 left (PB7L). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to PB7L. • Replace PB7L.

Table 19 ECUB detects I/O (EIOB) power fail

LED	Fault	Symptoms	Corrective action
58	Left Front I/O Board failure	1. 3.3V or 5V dropped below acceptable level (+12V and -12V not monitored). 2. Core utilities board (ECUB) detected a power loss on IOLF-iob_0_4 I/O board (EIOB). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to IOLF. • Replace I/O power board (EIOBPB). • Replace EIOB in left front.
59	Left Rear I/O Board failure	1. 3.3V or 5V dropped below acceptable level (+12V and -12V not monitored). 2. Core utilities board (ECUB) detected a power loss on IOLR-iob_1_5 I/O board (EIOB). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to IOLR. • Replace I/O power board (EIOBPB). • Replace EIOB in left rear.

Table 19 ECUB detects I/O (EIOB) power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
5A	Right Front I/O Board failure	1. 3.3V or 5V dropped below acceptable level (+12V and -12V not monitored). 2. Core utilities board (ECUB) detected a power loss on IORF-iob_3_7 I/O board (EIOB). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to IORF. • Replace I/O power board (EIOBPB). • Replace EIOB in RF.
5B	Right Rear I/O Board failure	1. 3.3V or 5V dropped below acceptable level (+12V and -12V not monitored). 2. Core utilities board (ECUB) detected a power loss on IORR-iob_2_6 I/O board (EIOB). 3. Core utilities board (ECUB) powers down the system.	• Replace 48V cable to IORR. • Replace I/O power board (EIOBPB). • Replace EIOB in RR.

Table 20 ECUB detects fan power fail

LED	Fault	Symptoms	Corrective action
5C	Fan failure Upper Right	1. Sensor in the upper right fan (as viewed from rear of system) determines fan failure.	• Replace upper right fan and fuse. • Check fan for loose connections.
5D	Fan failure Upper Middle	1. Sensor in the upper middle fan (as viewed from rear of system) determines fan failure.	• Replace upper middle fan and fuse. • Check fan for loose connections.
5E	Fan failure Upper Left	1. Sensor in the upper left fan (as viewed from rear of system) determines fan failure.	• Replace upper left fan and fuse. • Check fan for loose connections.
5F	Fan failure Lower Right	1. Sensor in the lower right fan (as viewed from rear of system) determines fan failure.	• Replace lower right fan and fuse. • Check fan for loose connections.

Table 20 ECUB detects fan power fail —**(continued)**

LED	Fault	Symptoms	Corrective action
60	Fan failure Lower Middle	1. Sensor in the lower middle fan (as viewed from rear of system) determines fan failure.	• Replace lower middle fan and fuse. • Check fan for loose connections.
61	Fan failure Lower Left	1. Sensor in the lower left fan (as viewed from rear of system) determines fan failure.	• Replace lower left fan and fuse. • Check fan for loose connections.

Table 21 ECUB detects ambient air error

LED	Fault	Symptoms	Corrective action
62	Ambient hot	1. Ambient air too hot. 2. Core utilities board (ECUB) powers down system. 3. Should have received "ambient air too warm" error 69 prior to this error.	• Check site temperature. • Verify ECUB settings with `ds1620`, if reoccurrence with site temperatures in spec. • Replace ECUB.
63	OVERTEMP ENRB	1. Node routing board (ENRB) too hot. 2. Core utilities board (ECUB) sensed overtemp on node routing board power board (ENRBPB) and powers down the system.	• Check the air filter, airflow blocked to ENRBPB. • Check fans. • Replace ENRBPB.

Table 21 ECUB detects ambient air error —**(continued)**

LED	Fault	Symptoms	Corrective action
64	QUADRL 0	1. Board overheated in Quadrant 0. 2. Core utilities board (ECUB) sensed overtemp in Quadrant 0 and powers down the system.	• Clean the filter, air blocked to one of the following boards. • Check fan lower left (as viewed from rear of system). • Isolate and replace the failing board by pulling boards from the following list. Right lower front • MB7R • PB6R • PB7R • IORF Right lower rear • MB6R • PB2R • PB3R • IORR

Table 21 ECUB detects ambient air error —**(continued)**

LED	Fault	Symptoms	Corrective action
65	QUADRU 1	1. Board overheated in Quadrant 1. 2. Core utilities board (ECUB) sensed overtemp in Quadrant 1 and powers down the system.	• Clean the filter, air blocked to one of the following boards. • Check fan upper left (as viewed from rear of system). • Isolate and replace the failing board by pulling boards from the following list. Right upper front • MB3R • PB5R • PB4R Right upper rear • MB2R • PB1R • PB0R

Table 21 ECUB detects ambient air error —**(continued)**

LED	Fault	Symptoms	Corrective action
66	QUADLL 2	1. Board overheated in Quadrant 2. 2. Core utilities board (ECUB) sensed overtemp in Quadrant 2 and powers down the system.	• Clean the filter, air blocked to one of the following boards. • Check fan lower right (as viewed from rear of system). • Isolate and replace the failing board by pulling boards from the following list. Left lower rear • MB4L • PB3L • PB7R Right lower front • MB5L • PB7L • PB6L

Table 21 ECUB detects ambient air error —**(continued)**

LED	Fault	Symptoms	Corrective action
67	QUADLU 3	1. Board overheated in Quadrant 3. 2. Core utilities board (ECUB) sensed overtemp in Quadrant 3 and powers down the system.	• Clean the filter, air blocked to one of the following boards. • Check fan upper right (as viewed from rear of system). • Isolate and replace the failing board by pulling boards from the following list. Left upper front • MB1L • PB4L • PB5L • IORF Left upper rear • MB0L • PB0L • PB1L • IOLR

Table 22 ECUB detects hard error

LED	Fault	Symptoms	Corrective action
68	Hard error (ERAC) (EPAC) (EMAC) (ETAC) (EPIC)	1. Hard error lines to core utilities board (ECUB) reported ASIC problem. 2. Bit and hard error bus determine which ASIC to check	• Read Error_log and replace ASIC. • See Chapter 13,"Errors and events".

Table 23 ECUB detects ambient air (intake) error

LED	Fault	Symptoms	Corrective action
69	Ambient air too warm is an environmental warning	1. Intake air through ECUB too warm.	• Check site temperature and correct. • Reset error with `pce_util`. • follow these steps, for reoccurrence with room temp in spec: – Verify ECUB settings with `ds1620` and `pce_util`. – Replace ECUB.

Table 24 ECUB detects dc error

LED	Fault	Symptoms	Corrective action
70	NPSUL failure (warning)	1. Node power supply upper left (Viewed from Node front) failure reported. 2. Low-priority error for redundant power configurations.	• Check upper left power supply seating. • Replace upper left power supply using warm swap procedure.
71	NPSUR failure (warning)	1. Node power supply upper right (Viewed from Node front) failure reported. 2. Low-priority error for redundant power configurations.	• Check upper right power supply seating. • Replace upper right power supply using warm swap procedure.
72	NPSLL failure (warning)	1. Node power supply lower left (Viewed from Node front) failure reported. 2. Low-priority error for redundant power configurations.	• Check lower left power supply seating. • Replace lower left power supply using warm swap procedure.
73	NPSLR failure (warning)	1. Node power supply lower right (Viewed from Node front) failure reported. 2. Low-priority error for redundant power configurations.	• Check lower right power supply seating. • Replace lower right power supply using warm swap procedure.

PWRUP states

The table below lists the PWRUP states applicable to the ATTN bit set to 0 and the system state.

Table 25 PWRUP state and associated boards

PWRUP state	Board powered on	Octant powered on
9	None	
8	ENRB	
7	ENRB plus octant	7
6	ENRB plus octants	7,6
5	ENRB plus octants	7,6,5
4	ENRB plus octants	7,6,5,4
3	ENRB plus octants	7,6,5,4,3
2	ENRB plus octants	7,6,5,4,3,2
1	ENRB plus octants	7,6,5,4,3,2,1
0	ENRB plus octants	7,6,5,4,3,2,1,0 (system all powered up)

The table below lists octant power section to physical board decode and associated processor numbers.

Table 26 Octant power description

Quadrant	Octant	Description	Boards	Processor number
3 LU	7 LUR	Left upper rear	IOLR, PB0L, PB1L, MB0L	PB0L = 0, PB1L = 3
	6 LUF	Left upper front	IOLF, PB4L, PB5L, MB1L	PB4L = 8, PB5L = 11
2 LL	5 LLR	Left lower rear	MB4L, PB3L, PB2L, (DTL)	PB3L = 7, PB2L = 4
	4 LLF	Left lower front	MB5L,PB7L,PB6L	PB7L = 15, PB6L = 12
1 RU	3 RUF	Right upper rear	PB5R, PB4R, MB3R, (DTR)	PB5R = 10, PB4R = 9
	2 RUR	Right upper front	PB1R,PB0R,MB2R	PB1R = 2, PB0R = 1
0 RL	1 RLF	Right lower rear	MB7R,PB6R,PB7R,IORF	PB6R = 12, PB7R = 14
	0 RLR	Right lower front	MB6R,PB2R,PB3R,IORR	PB2R = 5, PB3R = 6

JTAG status LEDs

The lower LEDs on the core utilities board (ECUB) indicate the JTAG status (68360 processor status). See Chapter 6,"System initialization faults" for the location of the JTAG LEDs. See the table below for the LED codes.

The number 3 LED is at the top, and the number 0 is on the bottom (0= LED off) (1= LED on).

Table 27 JTAG Debug LEDs

3 (top)	2	1	0	Firmware activity	Symptom	Action
0	0	0	0	Start		
Blink	0	0	1	Idle	Normal Status	
Blink	0	1	0	Panic	like a "Bus error" ping will fail	do_reset power cycle
Blink	0	1	1	Cop		
Blink	1	0	0	gdb		
Blink	1	0	0	Scan		
Blink	1	1	0	Core		

Memory board errors

11

Overview

This chapter discusses troubleshooting the Exemplar S-Class and X-Class servers memory related errors.

- Types of memory errors
- How to diagnose memory failures
- Utilities used with memory failures

Memory board errors

The most common failure during memory initialization is that some of the boards will fail, resulting in the following information displayed in the sppconsole window:

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
**** WARNING **** PB0R is installed but did not report in.
Initializing main memory.
  Probing memory: MB2R, MB3R, MB4L, MB5L
  **** WARNING **** Some or all of Main Memory was hardware deconfigured
  Initializing MB2R ........
  Initializing MB3R ........
  Initializing MB4L ........
  Initializing MB5L ........
Booting OBP.
OPB Power-On Boot on [0:0]
SPP2000, OBP Release 3.0.2, compiled 97/01/07 11:55:13
16 CPUs, 1972MB memory installed, 2PCI units available.
Complex Serial Number: -1, Node Serial Number 2011255.
Network address 0:a0:d9:0:b0:77, OBP IP Number 15.99.111.150.
Using sppux boot-mode
[0:0] ok
```

Use `dcm` to check which part of the memory board (EMB) is not coming up.

Note

For the following dcm script to work properly you must wait until you see `Database generation is complete` in the sppconsole window.

```
INFO: node id 0 was found
INFO: Database generation is complete
```

dcm utility

The dcm script looks for PERL code in /spp/bin/perl and reads, parses, and prints to the screen the boot configuration map in NVRAM through calls to sppdsh. The script usage is:

dcm *Node_number*

where *Node_number* is a hex value and the node on which to run dcm.

The following example runs dcm on nodes 0 and 4.

```
% dcm 0 4
```

The following example displays the dcm help file:

```
% dcm -h
```

Running dcm provides the following information:

- Checksum for Boot Configuration Map data structure
- Boot Configuration Map size
- POST revision version used to create the Boot Configuration Map
- Processor cache (instruction cache, data cache) size in MB
- Status of processor agent chip (EPAC) (PASS, FAIL, or EMPTY)
- Status of PCI-bus interface controller (EPIC) (PASS, FAIL, or EMPTY)
- Status of memory access chip (EMAC) (PASS, FAIL, or EMPTY)
- Status of toroidal access chip (ETAC) (PASS, FAIL, or EMPTY)
- Location of memory boards

POST sppconsole output with errors

The memory board and DIMM that has caused the problem will be identified by examining the dcm output.

The example POST sppconsole window output below illustrates where the error first occurs in POST.

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
**** WARNING **** PB0R is installed but did not report in.
Initializing main memory.
  Probing memory: MB2R, MB3R, MB4L, MB5L
  **** WARNING **** Some or all of Main Memory was hardware deconfigured
  Initializing MB2R........
  Initializing MB3R........
  Initializing MB4L........
  Initializing MB5L........
Booting OBP.
OPB Power-On Boot on [0:0]
SPP2000, OBP Release 3.0.2, compiled 97/01/07 11:55:13
16 CPUs, 1972MB memory installed, 2PCI units available.
Complex Serial Number: -1, Node Serial Number 2011255.
Network address 0:a0:d9:0:b0:77, OBP IP Number 15.99.111.150.
Using sppux boot-mode
[0:0] ok
```

dcm output example

The example output below of EMB 5 losing a row on DIMM B0S0 illustrates the resulting output of dcm.

Notice that the deconfigured DIMM that failed POST is marked as "EMPTY" and the other 15 DIMMS, marked as 16H00, have been automatically deconfigured due to one bad DIMM. DIMMS are deconfigured on a row by row basis.

```
% dcm 0
Excalibur Configuration Map Dump: Node: 0
        ========================================================
VERSION: 001.000.000.000          compiled: 1996/10/10 13:23:07   by: mullins
 Acquiring the Boot Configuration Map...
         Check Sum:              0xf1a83645
         Boot Config Map Size: 113 Words
         POST Revision:          1.7.0.0
 CPUs (ICache, DCache) Size in Bytes
 ===================================
 PB0L -       PASS (Unknown, Unknown)     PB0R -       PASS (Unknown, Unknown)
 PB1R -       PASS (Unknown, Unknown)     PB1L -       PASS (Unknown, Unknown)
 PB2L -       PASS (Unknown, Unknown)     PB2R -       PASS (Unknown, Unknown)
 PB3R -       PASS (Unknown, Unknown)     PB3L -       PASS (Unknown, Unknown)
 PB4L -       PASS (Unknown, Unknown)     PB4R -       PASS (Unknown, Unknown)
 PB5R -       PASS (Unknown, Unknown)     PB5L -       PASS (Unknown, Unknown)
 PB6L -       PASS (Unknown, Unknown)     PB6R -       PASS (Unknown, Unknown)
 PB7R -       PASS (Unknown, Unknown)     PB7L -       PASS (Unknown, Unknown)

 EPACs
 =====
 P0L -          PASS      P4L -          PASS
 P1R -          PASS      P5R -          PASS
 P2L -          PASS      P6L -          PASS
 P3R -          PASS      P7R -          PASS

 EPICs
 =====
 IOLF_B -       PASS      IOLF_A -       PASS
 IOLR_B -      EMPTY      IOLR_A -      EMPTY
 IORR_B -      EMPTY      IORR_A -      EMPTY
 IORF_B -      EMPTY      IORF_A -      EMPTY

 EMACs
 =====
 MB0L_M -       EMPTY     MB4L_M -       PASS
 MB1L_M -       EMPTY     MB5L_M -       PASS
 MB2R_M -       PASS      MB6R_M -       EMPTY
 MB3R_M -       PASS      MB7R_M -       EMPTY

 ETACs
 =====
 MB0L_T -      EMPTY      MB4L_T -      EMPTY
 MB1L_T -      EMPTY      MB5L_T -      EMPTY
 MB2R_T -      EMPTY      MB6R_T -      EMPTY
 MB3R_T -      EMPTY      MB7R_T -      EMPTY
```

```
Memory: B(ank#)S(lot#) - Row_0/Row_1
 ======= ============================
EMB2:
=====
B0S0 - 16MB/16MB   B0S1 - 16MB/16MB   B0S2 - 16MB/16MB   B0S3 - 16MB/16H00
B1S0 - 16MB/16MB   B1S1 - 16MB/16MB   B1S2 - 16MB/16MB   B1S3 - 16MB/16H00
B2S4 - 16MB/16MB   B2S5 - 16MB/16MB   B2S6 - 16MB/16MB   B2S7 - 16MB/16H00
B3S4 - 16MB/16MB   B3S5 - 16MB/16MB   B3S6 - 16MB/16MB   B3S7 - 16MB/16H00
EMB3:
=====
B0S0 - 16MB/16MB   B0S1 - 16MB/16MB   B0S2 - 16MB/16MB   B0S3 - 16MB/16H00
B1S0 - 16MB/16MB   B1S1 - 16MB/16MB   B1S2 - 16MB/16MB   B1S3 - 16MB/16H00
B2S4 - 16MB/16MB   B2S5 - 16MB/16MB   B2S6 - 16MB/16MB   B2S7 - 16MB/16H00
B3S4 - 16MB/16MB   B3S5 - 16MB/16MB   B3S6 - 16MB/16MB   B3S7 - 16MB/16H00

EMB4:
=====
B0S0 - 16MB/16MB   B0S1 - 16MB/16MB   B0S2 - 16MB/16MB   B0S3 - 16MB/16H00
B1S0 - 16MB/16MB   B1S1 - 16MB/16MB   B1S2 - 16MB/16MB   B1S3 - 16MB/16H00
B2S4 - 16MB/16MB   B2S5 - 16MB/16MB   B2S6 - 16MB/16MB   B2S7 - 16MB/16H00
B3S4 - 16MB/16MB   B3S5 - 16MB/16MB   B3S6 - 16MB/16MB   B3S7 - 16MB/16H00

EMB5:
=====
B0S0 - EMPTY/16MB  B0S1 - 16MB/16MB   B0S2 - 16MB/16MB   B0S3 - 16MB/16H00
B1S0 - 16MB/16MB   B1S1 - 16MB/16MB   B1S2 - 16MB/16MB   B1S3 - 16MB/16H00
B2S4 - 16MB/16MB   B2S5 - 16MB/16MB   B2S6 - 16MB/16MB   B2S7 - 16MB/16H00
B3S4 - 16MB/16MB   B3S5 - 16MB/16MB   B3S6 - 16MB/16MB   B3S7 - 16MB/16H00
```

For more information on `dcm` consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

mem3000

Many memory failures can be found using `est`; however, some require further investigation and the `mem3000` test.

Example of using `cxtest` in interactive mode to run `mem3000`

Step 1 Use the sppuser window to set the mode of the test controller to interactive mode and reset the system by typing

```
sppuser> /spp/scripts/tc_interactive
sppuser> do_reset
```

Below is the result in the sppuser window when booted in interactive mode.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
    0=Quit Test Controller
    1=Begin Test Controller Execution
    2=Halt Test Controller Execution
    3=Resume Test Controller Execution
    4=Switch CPU
    5=POST Boot selection
    6=Execution Mode Selection
    7=Global Parameter Display
    8=CPU Summary Display
    9=Display CPU Errors
    A=Test Selection Menu
    B=Test Configuration Menu
    C=Debugging Menu
    D=Display Revision
Enter command:
```

Step 2 In the sppuser window, set up the test controller for selection of a particular test.

```
Enter command: A
```

Step 3 From the Test Selection Menu enter:

```
    1=Memory test
    2=Archetecture Features test
    3=Intra-Node Coherency test
    4=Inter-node Coherency test
    5=I/O test
    6=CPU Selftests
Please enter number of test: 1
```

Step 4 Return to the Main Menu.

```
    Enter command: 0
```

Step 5 Select the Test Configuration Submenu.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: B
```

Step 6 From the Test Selection Menu enter:

```
   1=Memory test
   2=Archetecture Features test
   3=Intra-Node Coherency test
   4=Inter-node Coherency test
   5=I/O test
   6=CPU Selftests
Please enter number of test: 1
```

Step 7 In the Test Configuration Menu, enter option 4

```
Test Configuration Menu
   0=Return to Main Menu       9=Display Test Parameters
   1=Display Classes           A=Hardware Selection Menu
   2=Display Subtest           B=Loop Enable
   3=Select Classes            C=Loop Count
   4=Select Subtests           D=Test Error Count
   5=Read All Test Parameters  E=Pause at Test Start
   6=Read One Test Parameter   F=Pause at Test End
   7=Write Test Parameter      G=Pause at Subtest Start
   8=Reset Parameters          H=Pause at Subtest End
Enter command: 4
```

Step 8 Enter the subtest or subtest range (usually 110, 130, 150 and 155 are the most useful memory tests).

```
Enter the subtest number or subtest range: 110
```

Step 9 Determine the type of DIMM (80 or 88 bit) used by physically inspecting the DIMMS.

Step 10 Enter the Size (80 or 88 bit) DIMMS in option 7 of the Test Configuration Submenu.

```
Test Configuration Menu
    0=Return to Main Menu       9=Display Test Parameters
    1=Display Classes           A=Hardware Selection Menu
    2=Display Subtest           B=Loop Enable
    3=Select Classes            C=Loop Count
    4=Select Subtests           D=Test Error Count
    5=Read All Test Parameters  E=Pause at Test Start
    6=Read One Test Parameter   F=Pause at Test End
    7=Write Test Parameter      G=Pause at Subtest Start
    8=Reset Parameters          H=Pause at Subtest End
Enter command: 7
```

Step 11 Specify the test parameter to write to (use parameter 6).

Step 12 Enter the new value for the test parameter (1 for 88 bit DIMMS).

Step 13 Return to the Main Menu.

```
Enter command: 0
```

Step 14 From the Main Menu, begin the Test Controller.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
    0=Quit Test Controller
    1=Begin Test Controller Execution
    2=Halt Test Controller Execution
    3=Resume Test Controller Execution
    4=Switch CPU
    5=POST Boot selection
    6=Execution Mode Selection
    7=Global Parameter Display
    8=CPU Summary Display
    9=Display CPU Errors
    A=Test Selection Menu
    B=Test Configuration Menu
    C=Debugging Menu
    D=Display Revision
Enter command: 1
```

The sppuser window displays the following message.

```
Execution Starting.
.............
.............
Execution Complete
```

Main Menu comes up again.

Step 15 To see the results of the test, select the CPU summary option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 8
```

This command shows if the test passed or failed, as shown in the following examples.

```
Configuration Map (shows the arrays and cpu's enabled)
CPUs:0 1 2 3 4* 5 6 7 8 9 A B C D E F
EPACs:0*1*2*3*4*5*6*7* EPACs:0*1*2*3*4*5*6*7*

 CPU STATE            FAIL      SUBTEST      TEST NAME
                      COUNT

 ==  =====            =====     ======       ========

 0   Not Available    n/a       n/a          n/a

 4   Error Detected   1         110          MEM3000 - EEPROM based memory tests

 F   Not Available    n/a       n/a          n/a
```

Step 16 To see how the test failed, select the Display CPU option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 9
```

Step 17 Enter the number of the CPU that failed to show how the test failed.

```
Enter CPU [0-f]: 4

 Date/Time  hh:mm:ss   SUBTEST   Event       Error
  mm/dd/yy                      Code        Message

 ========  ========   =======   ========    ========

 03/03/97   14:06:55   110       866b1020    MB0L_M/B0S0/0000000000/30000001/20000
                                              001/

 00/00/00   00:00:00          0  00000000

 00/00/00   00:00:00          0  00000000

 00/00/00   00:00:00          0  00000000
```

Step 18 For the field definitions for the event code and error message, perform `man mem3000` to determine the meaning of the error messages.

To accurately determine if the failure is the Exemplar Memory Board (EMB) or the DIMM many times the reported DIMM or row is just the first one the test found. Because of this and the layout of the Exemplar Memory Board it is often necessary to isolate all the failing rows to get a total picture of the failure. By manipulating the `cxtest` parameters, the test can be made to test one row or one bank at a time while running the failing subtest.

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `mem3000` utility.

Processor errors

12

Overview

The chapter covers troubleshooting the system processor errors related to the processor boards.

- Processor errors
- Types of processor errors
- Diagnosis of processor errors
- Utilities

Common processor errors

Common failures encountered for processor related problems are listed in Table 28.

Table 28 Common processor failures

Error	Corrective action
`**** WARNING ***` `PB4L is installed but did not report in`	System probing for CPUs during POST get this message. • Check for bad solder connection at the runway bus clock sockets. • Check clock at feed through on the opposite side of the node routing board (ENRB). • Check CPU in message: it must be plugged in. • Check for a bad processor agent chip (EPAC) or gate array socket, verify this with `est` diagnostic.
`****WARNING ***` `PB1L is idle but timed out during ping operation`	Check runaway bus delay line is plugged all the way in it's socket on the node routing board (ENRB).
System fails to margin to lower power.	• Look for bad solder connection on the node routing board (ENRB). • EMI filters sometimes do not reflow leaving an open GND or +48V signal on the pcb.

cpu3000 test

Most CPU failures can be found using est; however, some require further investigation with the cpu3000 test.

Example of using cxtest in interactive mode to run cpu3000

Step 1 In the teststation window, set the mode of the test controller to interactive mode and reset the system.

```
sppuser> /spp/scripts/tc_interactive
sppuser> do_reset
```

Below is the result in the teststation window when booted in interactive mode.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command:
```

Step 2 In the sppuser window, set up the test controller for selection of a particular test by entering the command:

```
Enter command: A
```

Step 3 From the Test Selection Menu enter:

```
1=Memory test
2=Archetecture Features test
3=Intra-Node Coherency test
4=Inter-node Coherency test
5=I/O test
6=CPU Selftests
Please enter number of test: 6
```

Step 4 Return to the Main Menu.

```
Enter command: 0
```

Step 5 Select the Test Configuration Submenu.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: B
```

Step 6 From the Test Selection Menu enter:

```
1=Memory test
2=Archetecture Features test
3=Intra-Node Coherency test
4=Inter-node Coherency test
5=I/O test
6=CPU Selftests
Please enter number of test: 6
```

Step 7 In the Test Configuration Submenu, select 4.

```
Test Configuration Menu
   0=Return to Main Menu       9=Display Test Parameters
   1=Display Classes           A=Hardware Selection Menu
   2=Display Subtest           B=Loop Enable
   3=Select Classes            C=Loop Count
   4=Select Subtests           D=Test Error Count
   5=Read All Test Parameters  E=Pause at Test Start
   6=Read One Test Parameter   F=Pause at Test End
   7=Write Test Parameter      G=Pause at Subtest Start
   8=Reset Parameters          H=Pause at Subtest End
Enter command: 4
```

Step 8 Enter the subtest or subtest range.

```
Enter the subtest number or subtest range: 100-300
```

Step 9 Return to the Main Menu.

```
Enter command: 0
```

Step 10 From the Main Menu, begin the test controller.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 1
```

The teststation window displays the follwing message.

```
Execution Starting.
.............
.............
Execution Complete
```

Main Menu comes up again.

Step 11 To see the results of the test, select the CPU summary option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 8
```

This shows if the test passed or failed.

```
CPU  STATE     FAIL      SUBTEST       TEST NAME
                COUNT

==   =====     =====     ======        ========

2    Failed    0         200           CPU3000 -EEPROM based CPU tests
```

Step 12 To see how the test failed, select the Display CPU option.

```
Booting DIAGS
SPP2000 Test Controller, version 1.4.0.0, compiled 1996/11/22 11:46:10
   0=Quit Test Controller
   1=Begin Test Controller Execution
   2=Halt Test Controller Execution
   3=Resume Test Controller Execution
   4=Switch CPU
   5=POST Boot selection
   6=Execution Mode Selection
   7=Global Parameter Display
   8=CPU Summary Display
   9=Display CPU Errors
   A=Test Selection Menu
   B=Test Configuration Menu
   C=Debugging Menu
   D=Display Revision
Enter command: 9
```

This command shows how the test failed.

```
Enter CPU [0-f]: 4

 Date/Time  hh:mm:ss   SUBTEST   Event      Error
  mm/dd/yy                      Code       Message

 =========  ========   =======   ========   ========

 03/03/97   14:06:55   310       80c43219   T:64120/2bffffff:c0000000/53ffffff:c0
                                             000000
```

Step 13 To determine what the error message means, use the mouse to select or copy the whole line containing the error message.

Step 14 In the tsch window type the following command:

```
cpu3000_decode
```

Step 15 Paste the error message after this command and hit return for a list of suspect SRAMs.

Consult the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020) for more information on the `cpu3000` utility.

Errors and events 13

Overview

The chapter covers troubleshooting the system using the message and sppconsole windows:

- Message window
  - Log files
  - Hard errors
  - Advisory errors
- Sppconsole window
  - SPP-UX log files
  - SPP-UX soft ECC errors, both memory and CPU cache

Message window

The message window on the teststation actively displays errors and/or events as they occur. There are files on the teststation that are used to log errors, located in the `/spp/data` directory. Table 29 lists the name of the file and a description of what the file contains.

Table 29 Log Files

Filename	Description
`event_log`	Main file used for logging everything
`hard_hist`	Filtered output from the hard_logger, appended to after each error. It contains a complete list of hard errors. Use **SHIFT-G** when viewing the files.

Hard errors

A hard error is an error that prevents returning an error response or corrupts data so that future references cannot detect the corruption. An example is a parity error detected on the address of a memory transaction. The appropriate memory line cannot be updated, and future consumers of the lines are not notified of the corruption.

If a hard error occurs while the node is in OS, it will crash the node. The system must then be rebooted after the cause has been determined. There are many different kinds of error messages that a node can pull, but the general process is summarized below.

A hard error is sent to the monitoring utilities board (EMUC) and processor utilities chip (EPUC) on the core utilities board, which generates an HPMC (High Priority Machine Check) to one of the processors. All error CSRs (Control and Status Registers) are locked so that additional errors are not logged.

Note

In the event that more than one device generates a hard error, the software can determine which device generated it first, through the use of the CSRs and Data Extractors (scripts that read the appropriate data and piece it together).

When the hard error occurs, the following results:

- Attention LEDs flash.
- Clocks stop so that data in CSRs is preserved.
- Script hard_logger is invoked to log the error information from the node through the JTAG (scan) interface.

Hard error output appears in the sppuser window. This information is also written to the event log at `/spp/data/event_log` so that it can be reviewed.

Note

Because the cause of a hard error may not be the part that reported it, it is important to have a good understanding of the architecture of the node, so that the source and destination of the failing data can be understood.

For information on the architecture of the node refer to the *Exemplar Architecture Reference Manual: S-Class and X-Class Servers* (A4716-90001)

For information on the operation of the `hard_logger` type `man` *topic* in the sppuser window. Also refer to the *Exemplar Diagnostics Guide: S-Class and X-Class Servers* (A4716-90020).

Example of a hard error

OBP errors occur during initialization and can show up as hard errors because POST passes. The server appears to hang while booting the OBP module.

In most cases, the following occur.

1. The output from powerup appears in the sppconsole window.

```
SPP2200, POST version 1.1.2.0, compiled 1997/03/05 12:45:56
Monarch: PB0L
Initializing main memory.
  Probing memory: MB2R, MB3R, MB4L, MB5L
  Initializing MB2R ........
  Initializing MB3R ........
  Initializing MB4L ........
  Initializing MB5L ........
Booting OBP.
OPB Power-On Boot on [0:0]
```

2. The front panel LCD indicates that a CPU Trap on a processor has occurred. An example is shown below.

3. After a few seconds the Attention LEDs flash.
4. Shortly after these steps occur, the output from the hard_logger (information collected about the hard error) scrolls in the sppuser window as shown in the example below.

```
*** questioning suspect: erac[1]
** Erac 1 needs to be interrogated:
          its hard error group pin indicates
          that only this chip was the first to encounter this error
================================================================================
erac_interrogator is running on NODE n0 ERAC r11

error_cause          = 0x3e
error_info           = 0x665a
error_config         = 0x1db
error_group          = 0x0
--------------------------------------------------------------------------------
hard error Group bit = 0x0 The ERAC's hard error pin WAS NOT driven
                           by another chip.
error_info phase     = 0xd
error_info S         = 0x0
```

```
------------------------------------------------------------------------------
error_cause register indicates 5 error (s):
bit    severity    error name
---    --------    ----------
 0     advisory    Latch Array Read Parity Error
 1       hard      Input Queue Overflow
 2       hard      Input Parity Error on Critical Cycle
 3     advisory    Input Parity Error on Non-Critical Cycle
 4       hard      Null Route Mask
*EX!*     Running extractor r_queue_over_error n0:21:internal:r11 m2:
Event Code = 0xf00
------------------------------------------------------------------------------
NODE 0 ERAC R1L PORT M2 detected a Input Queue Overflow Error
     r_la_hold                      = 0
     c_queue_over                   = 1* error was detected
     Scan Fields
------------------------------------------------------------------------------
     core.r_err_cause [0:6]         = 3e
     core.r_err_info [1:15]         = 6642
     la0.r_di[0:31]                 = ec0a4a00
     la0.r_wr_ad[0:5]               = 3d
     la0.r_we                       = 0

     ERAC Port                      = EMAC 2
     Packet Source                  = EMAC MB5L
```

5. The output calls out the error in the `Packet Source` section of the file as a problem with the ERAC detecting an error from data sent from the EMAC on the memory board MB5L.

Run `est` to verify the scan ring passes.

Advisory errors

There is a second type of error called advisory errors that are similar to hard errors. An advisory error is different in that data is corrupted, like a hard error, but future references can detect the corruption, whereas hard errors cannot be detected by future references.

Sppconsole window

The console window on the teststation actively displays errors and/or events as they occur. There are also files generated from this window, which can also be viewed from the `/spp/data` directory. Table 30 lists the name of the file and a description of what the file contains.

Table 30 Configuration and log files

Filename	Description
`consolelog`	Complete log of all input/output in the sppconsole window.
`est.log`	Log file for the `est` program
`cxtest.log`	Log file for the `cxtest` diagnostic interface
`node-[#].cfg`	Configuration file for each node that contains board and ASIC information only for parts installed in the system

Soft errors

Soft errors are usually single-bit correctable errors that occur in SPP-UX. Through the use of an ECC code stored with the data, the memory subsystem is able to detect and correct single bit errors.

OS boot soft error

The following is example output of a soft error that occurred during the OS boot. This section explains how to troubleshoot this error.

```
[0:3]*****Received EMAC error notification interrupt.
[+8 72000001 002814f0 0:3]
EMAC #0 [0-7]
EMAC Chip Config: (0x00de20000061000) :PartNum de, Vers,Is 0
EMAC Error Cause: (0x000002000000000) : HarderrGrp 0,XbarPort 0
   LaInOverXbarPort 0,LaOutUnderXbarPort 0,LaInOver# 0,LaOutUnder# 0
   ErrBits 0x0000020000000000
   ->'Single Bit Memory Data ECC Error'
EMAC Error Info: (0x400c40402030355848) : ErrType 1, Overwritten 0
->Multiple 0, Synd 62 Enum 1, XbarPort 0,Responseless 0
->Errinfo 101aac2,Phase 4, Simult 0
->ErrType 'Advisory Error',ErrNum'Single Bit DataEcc Error'
EMAC Error Address-0x0000f600981eaba0
->MemRef: V1 0xf6, Node 0x0, Rw 1, VR 1, Vb2
->MemRef: Page 0x1ea,PgOfs ox5d,Bankbit 0,Even_Odd 0,Low_High 0
->Bank Referenced: 0
```

Step 1 Decode RAM causing the soft error with the script.

```
/spp/script/soft_decode.
```

Step 2 Determine failing Exemplar Memory Board (EMB) as in `EMAC #0` above.

Step 3 Determine type of failure found above by decoding the ErrBits to Single Bit Data ECC Error.

Step 4 Determine the failing DIMM by using the bank referenced field above.

Dcache soft errors on a processor

The dcache parity errors look like the following:

```
[0:3] cpu 10 dcache parity hpmc at 0x0000000000007c37:0x000000008fc
[0:3] pid 80 (test005)
[0:3] DR2=0x020500000004002
[0:3] RDR20 0xffffffffffff000000 0x000000000000000 0x00000000000001
[0:3] RDR21 0xffffffffffff000000 0x000000000000000 0x00000000000001
```

Use the executable script called `/users/sppuser/script/dc` to determine which SRAMs are suspect.

`dc` *RDR#*

Use the last two bits of RDR, not last two nibbles.

From above example, the *RDR#* would be **`dc 20 01.`**

The processor board can be rejected at this point

Icache soft errors on a processor

The Icache parity errors look like the following:

```
[+479 72000001 003096b4 0:f]Icache Parity Error:TimeTOC 0x000000002caa0760,
ParityBit Icache word2
[+479 72000001 003096f0 0;f] RDR1 0x558055805580, RDR3 0x000000000000000
0x0000000008000000
```

This Icache parity error can be a real error, or it can be caused by `ccmd` losing contact with the server. If `ccmd` loses contact, then you will see a `ccmd` error in the teststation console like the following:

```
ccmd:node detection complete Mon Apr 28 18:03:34 1997
ccmd:node detection complete Mon Apr 28 18:03:34 1997
ccmd:node detection complete Mon Apr 28 18:03:34 1997
ccmd:No nodes were detected - waiting.
ccmd:node detection complete Mon Apr 28 18:03:34 1997
ccmd:node id0 was found.
```

In the event the soft error was real, determine the SRAM that is suspect by executing the `ic` script.

`sppuser>` **`/users/sppuser/script/ic`** *word#/#*

The value of *word#/#* would be **`2`** in the above example.

The processor board with the suspect SRAM can be rejected at this point.

Component removal and replacement 14

Overview

This chapter describes the removal and replacement of the identified Field Replaceable Units (FRU). Procedures describe the step-by-step process required to safely remove or replace a component. Information about the hazards associated with the process are emphasized to prevent injury to personnel or damage to a component.

All steps must be completed in the order described. Any deviation from these steps could render the system inoperable or cause internal damage to the system.

Removal and replacement preliminary tasks

The following actions must be accomplished prior to removing and/or replacing any server component.

- Power down the system
- Remove the appropriate skins
- Remove the EMI panels

PCI cardcage

The following sections provide the information required to remove and install the PCI cardcage.

Removal

This section provides the details required to remove the PCI cardcage.

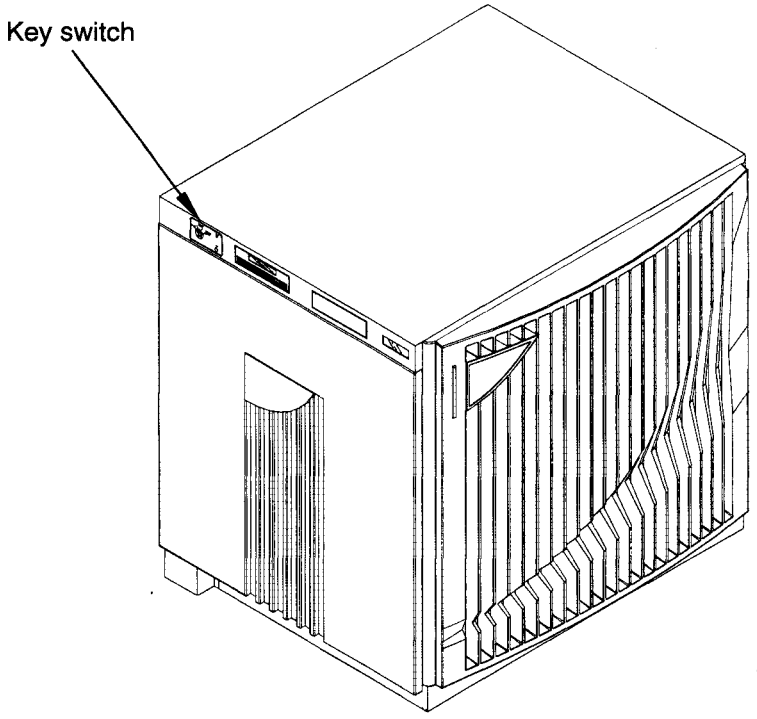
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the *shutdown* man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **DC OFF** position. Refer to Figure 17 for keyswitch location.

Figure 17 Keyswitch location



Note

Turn off power to the system before you remove the PCI cardcage. Failure to remove power before removing the PCI cardcage will damage electronic components on the board assembly.

Step 3 Select the PCI cardcage you intend to remove. The chassis can contain from one to four PCI cardcages, depending on your system configuration. The PCI cardcage you are targeting determines which side skin you need to remove. Refer to Figure 18 for possible locations of PCI cardcages in the chassis. Refer to Figure 19 for location of the PCI cardcage indicated by a specific LCD panel failure code.

Figure 18 PCI cardcage locations

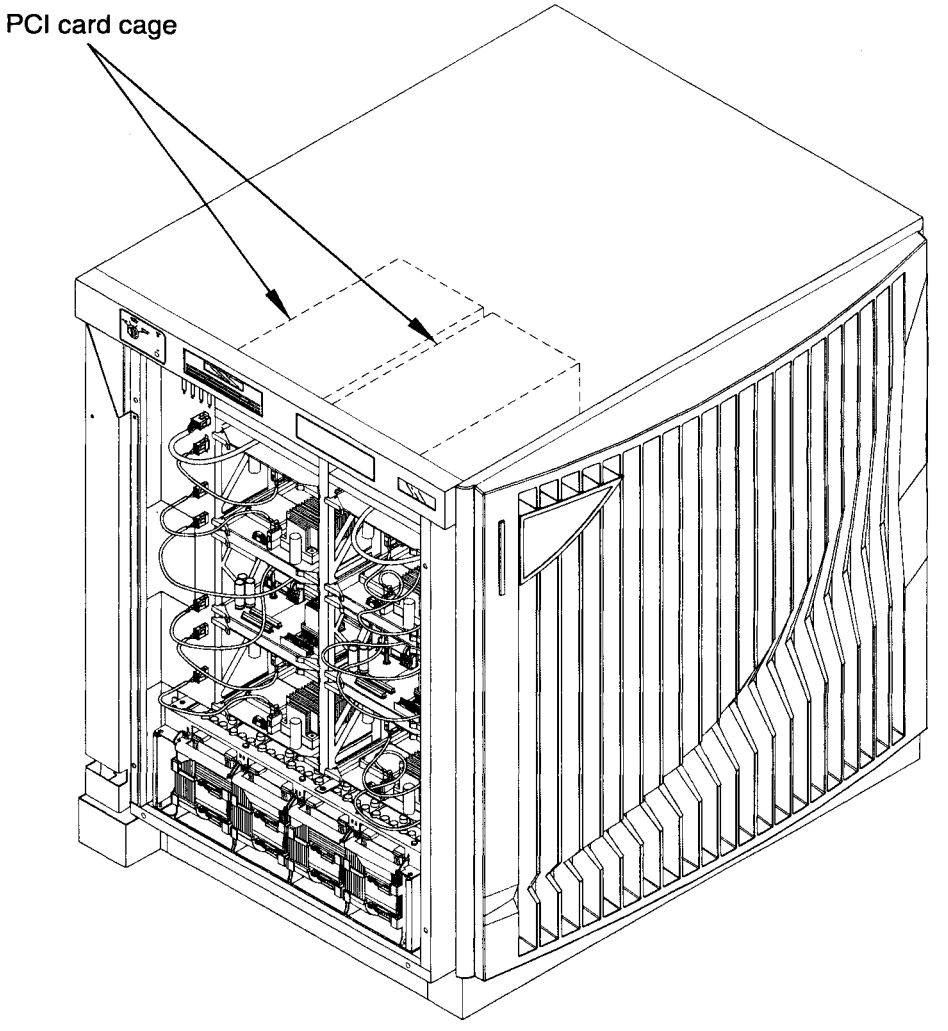
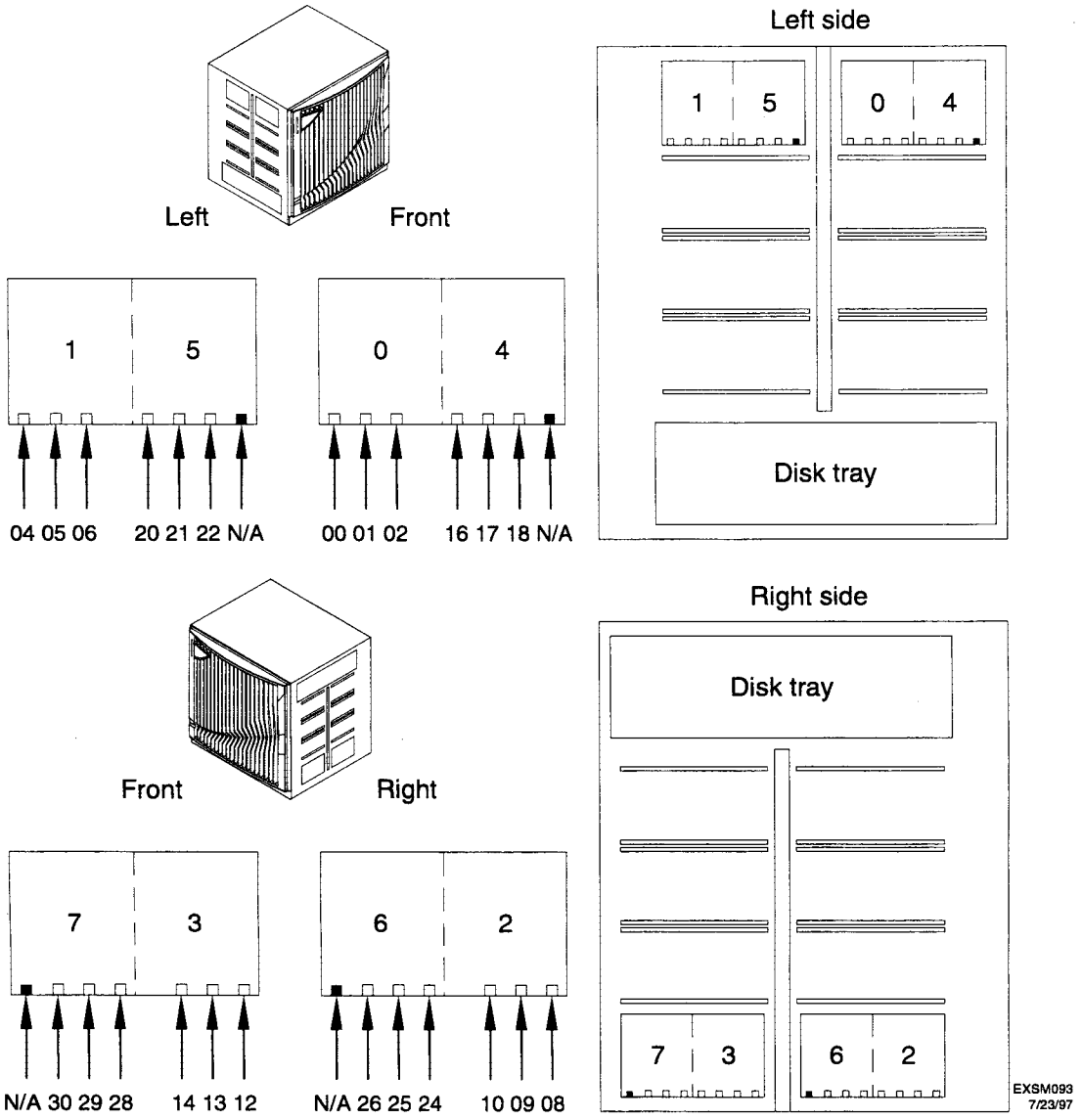
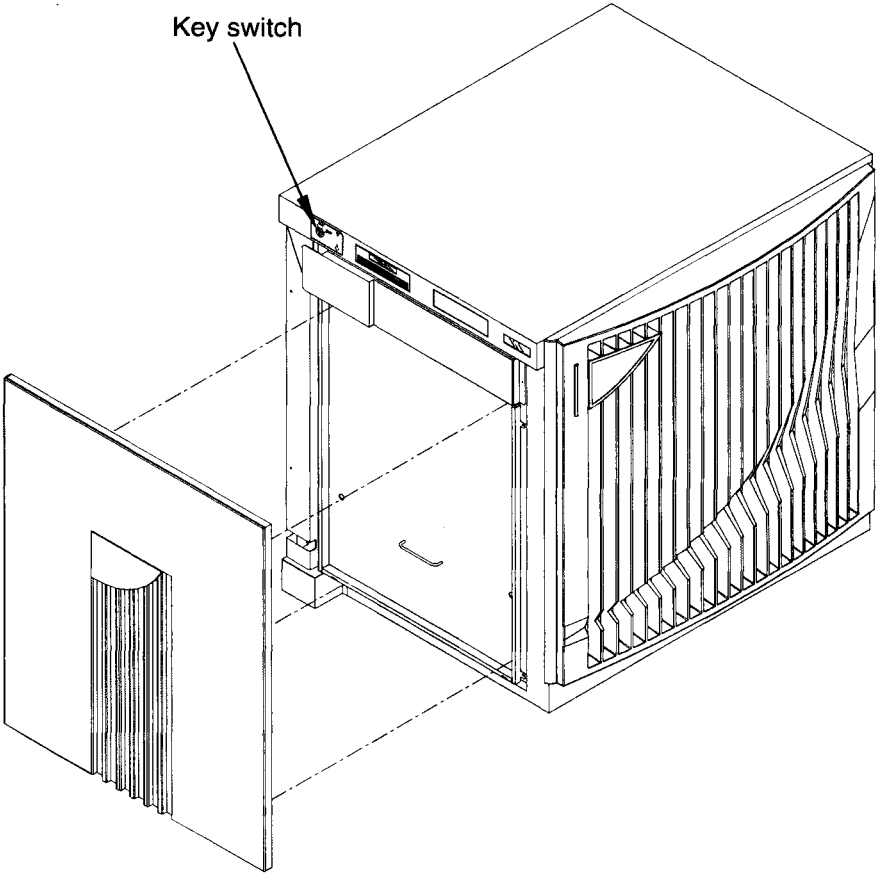


Figure 19 PCI cardcage location by failure code



Step 4 Remove the applicable side cabinet skin by pulling from the top and bottom of the skin until it pops out. Each skin has a set of four catch pins securing it to the chassis. Refer to Figure 20 for details.

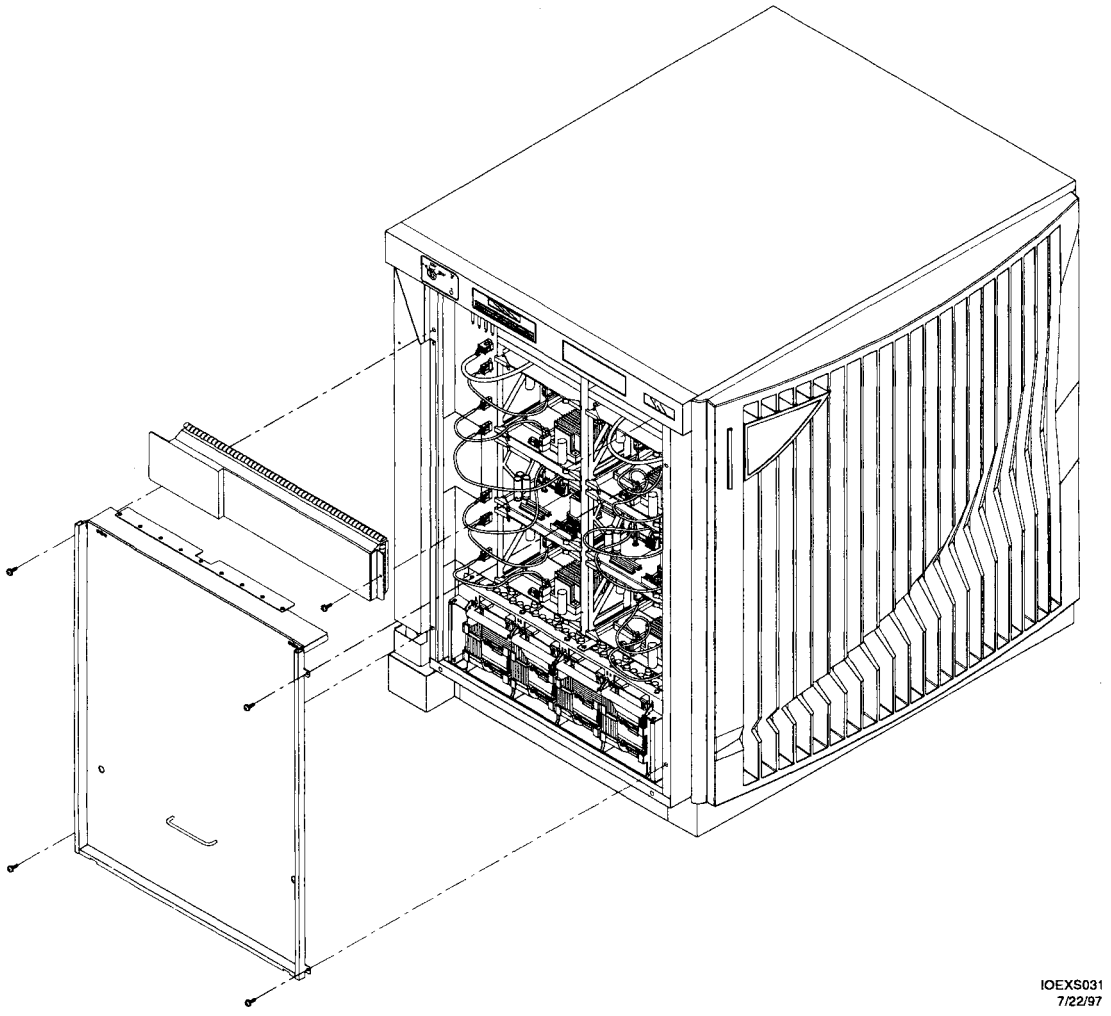
Figure 20 Side skin removal



Step 5 Remove the upper EMI panel by removing the screw that fastens the panel to the chassis. Refer to Figure 21 for details.

Step 6 Remove the lower EMI panel by removing the four screws that fasten the panel to the chassis. Refer to Figure 21 for details.

Figure 21 EMI panel removal



Step 7 Remove upper circuit board card retainer. Loosen two screws securing retainer to the chassis.

Step 8 Unplug the power cable on the front of the target PCI cardcage. The power connections are labeled on the chassis and are designated as follows:

IOLF—I/O Left Front

IOLR—I/O Left Rear

IORF—I/O Right Front

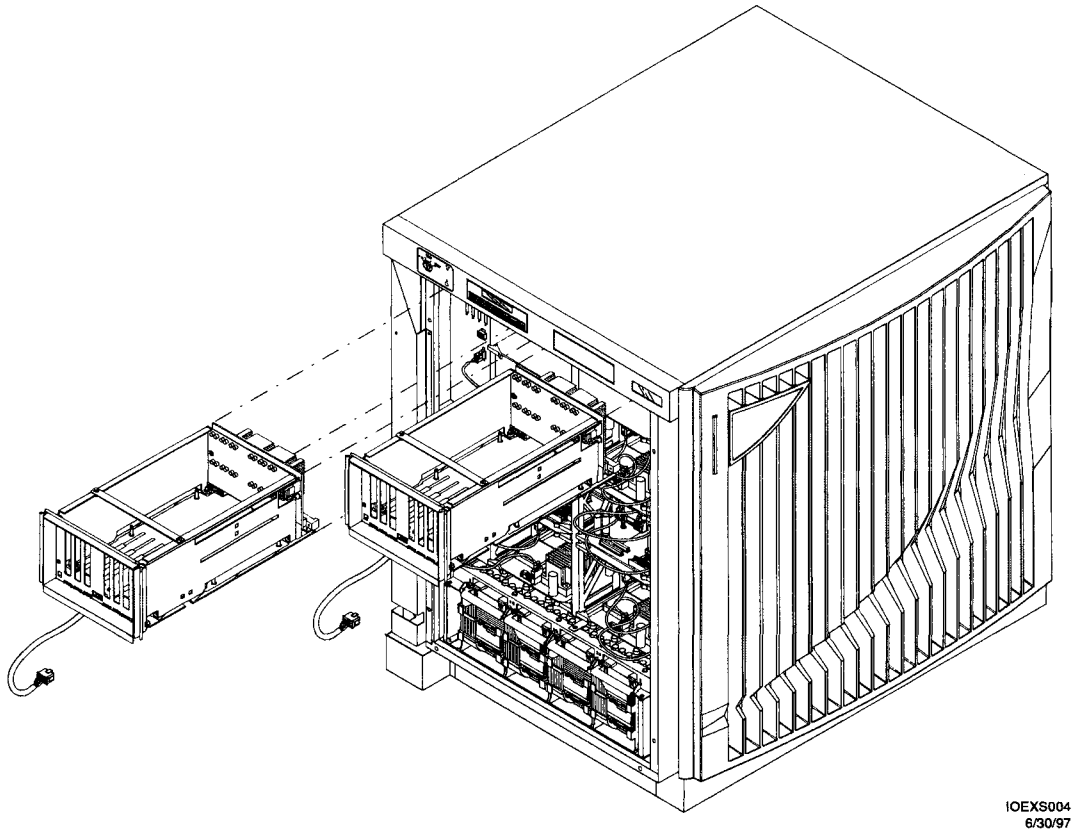
IORR—I/O Right Rear

Step 9 Disconnect all SCSI and network cables attached to controllers in the PCI cardcage. Mark or chart the connections for easy connection later.

Step 10 Remove the PCI cardcage from the chassis by pulling the two extractor levers on the front of the PCI cardcage toward you until the PCI cardcage is unseated from the node routing board (ENRB). Continue sliding the PCI cardcage all the way out, taking care to support it underneath. Refer to Figure 22 for PCI cardcage removal details.

Step 11 Place the cardcage on a static free, level work surface.

Figure 22 PCI cardcage removal



Installation

This section provides the details required to install the PCI cardcage.

Step 1 Install the PCI cardcage into the chassis by lining up the PCI cardcage with the guide rails. Continue sliding the PCI cardcage into the chassis and secure it using the two extractor levers.

Step 2 Connect the power cable from the PCI cardcage to the chassis.

Step 3 Attach any cables disconnected during removal to their proper locations.

Step 4 Install the top circuit card retainer. Secure two screws to the chassis.

Step 5 Install the lower EMI panel. Use four screws.

Step 6 Install the upper EMI panel. Use one screw.

Step 7 Install the skin.

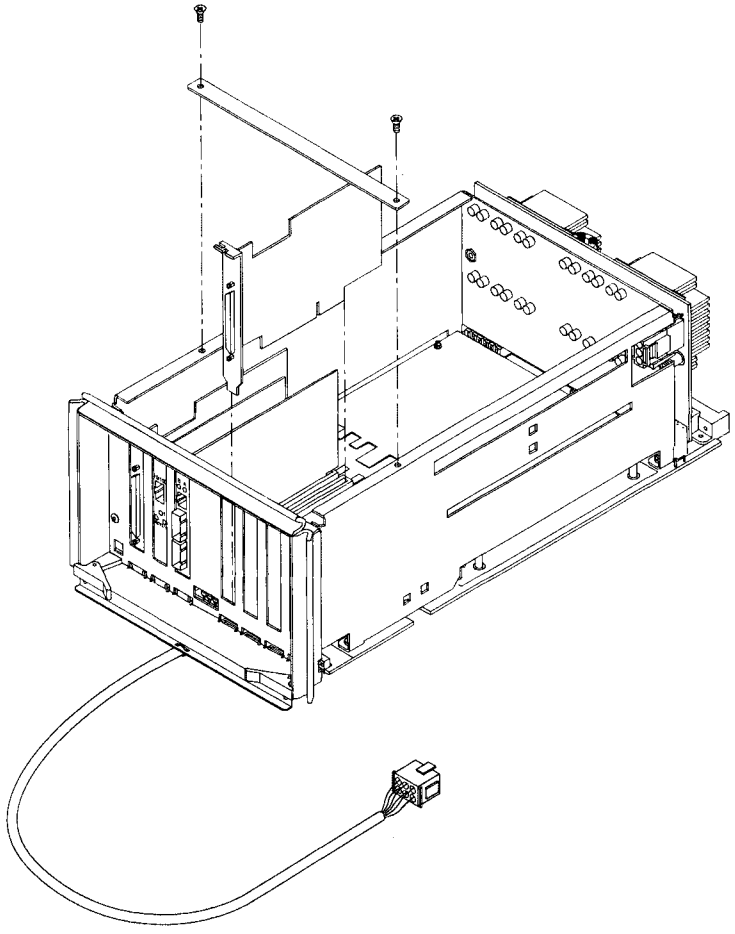
SCSI controller

This section provides the details required to remove and install the SCSI controller

Removal

This section provides the details required to remove the SCSI controller. Refer to Figure 23 for SCSI controller removal details.

Figure 23 SCSI controller removal



Step 1 Remove the two screws that secure the bracket to the top of the cardcage.

Step 2 Remove the screw on the faceplate of the PCI SCSI controller. Retain the screw for later use.

Step 3 Remove the controller by grabbing the edges of the board and pulling upward until the controller is free from the PCI connector.

Installation

This section provides the details required to install the SCSI controller.

Note

Verify that the faceplate of the card to be installed is centered in the chassis opening and secure against the front of the chassis gasket before installing the screw in the faceplate.

Step 1 Insert the new controller in the slot just vacated. Secure in position by installing the screw in the faceplate.

Step 2 Install the bracket on the top of the PCI cardcage. Attach with two screws.

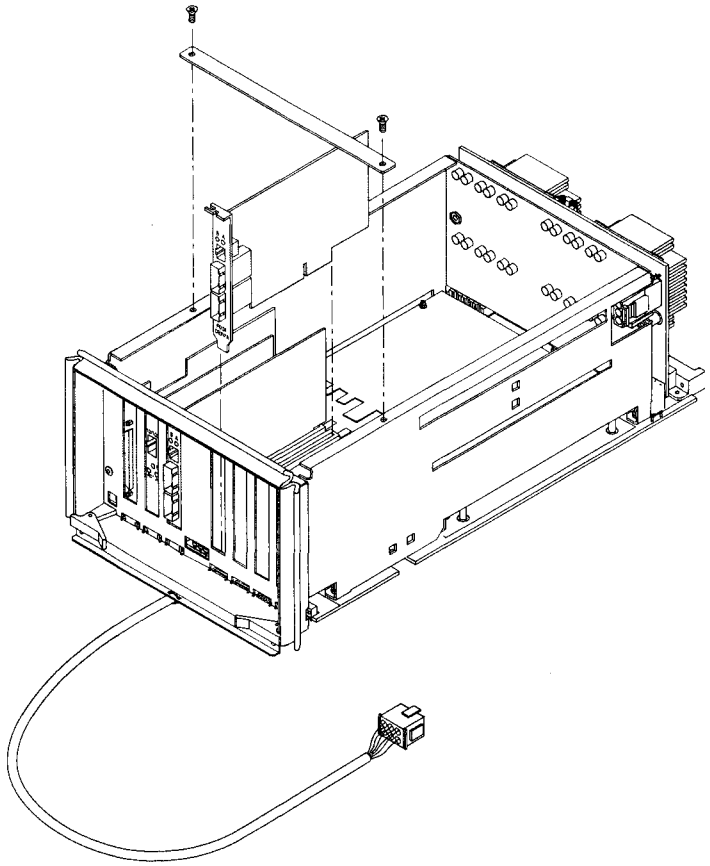
FDDI controller

This section provides the details required to remove and install the FDDI controller.

Removal

This section provides the details required to remove the FDDI controller. Refer to Figure 24 for FDDI controller removal details.

Figure 24 FDDI controller removal



Step 1 Remove the two screws that secure the bracket to the top of the cardcage.

Step 2 Remove the screw on the faceplate of the FDDI controller. Retain the screw for later use.

Step 3 Remove the controller by grabbing the edges of the board and pulling upward until the controller is free from the PCI connector.

Installation

This section provides the details required to install the FDDI controller.

Note

Verify that the faceplate of the card to be installed is centered in the chassis opening and secure against the front of the chassis gasket before installing the screw in the faceplate.

Step 1 Insert the new controller in the slot just vacated. Secure in position by installing the screw in the faceplate.

Step 2 Install the bracket on the top of the PCI cardcage. Attach with two screws.

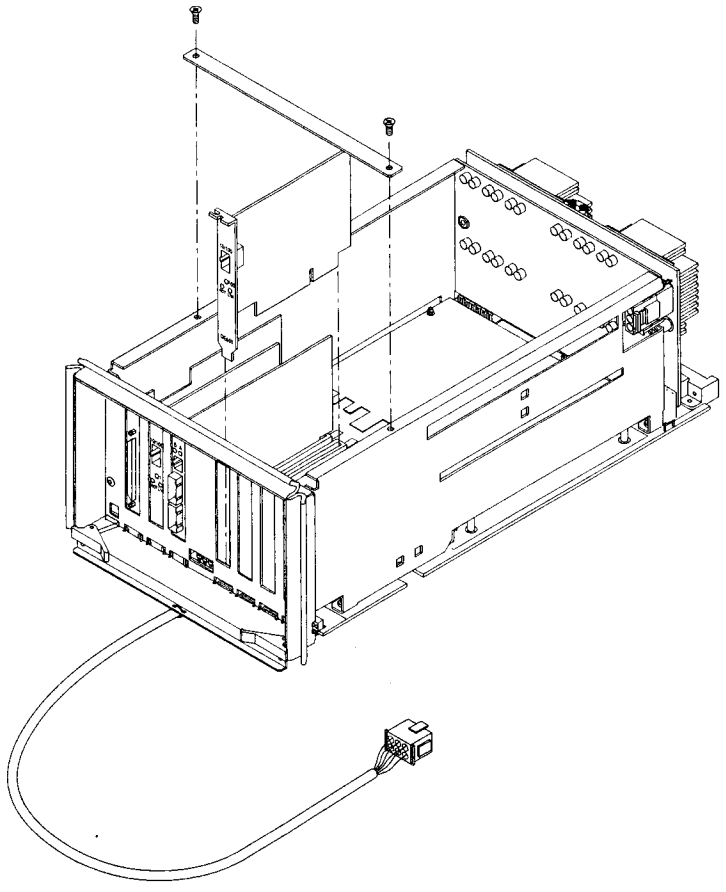
Fast Ethernet

This section provides the details required to remove and install the Fast Ethernet controller.

Removal

This section provides the details required to remove the Fast Ethernet controller. Refer to Figure 25 for Fast Ethernet controller removal details.

Figure 25 Fast Ethernet controller removal



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Step 1 Remove the two screws that secure the bracket to the top of the cardcage.

Step 2 Remove the screw on the faceplate of the Fast Ethernet controller. Retain the screw for later use.

Step 3 Remove the controller by grabbing the edges of the board and pulling upward until the controller is free from the PCI connector.

Installation

This section provides the details required to install the Fast Ethernet controller.

Note

Verify that the faceplate of the card to be installed is centered in the chassis opening and secure against the front of the chassis gasket before installing the screw in the faceplate.

Step 1 Insert the new controller in the slot just vacated. Secure in position by installing the screw in the faceplate.

Step 2 Install the bracket on the top of the PCI cardcage. Attach with two screws.

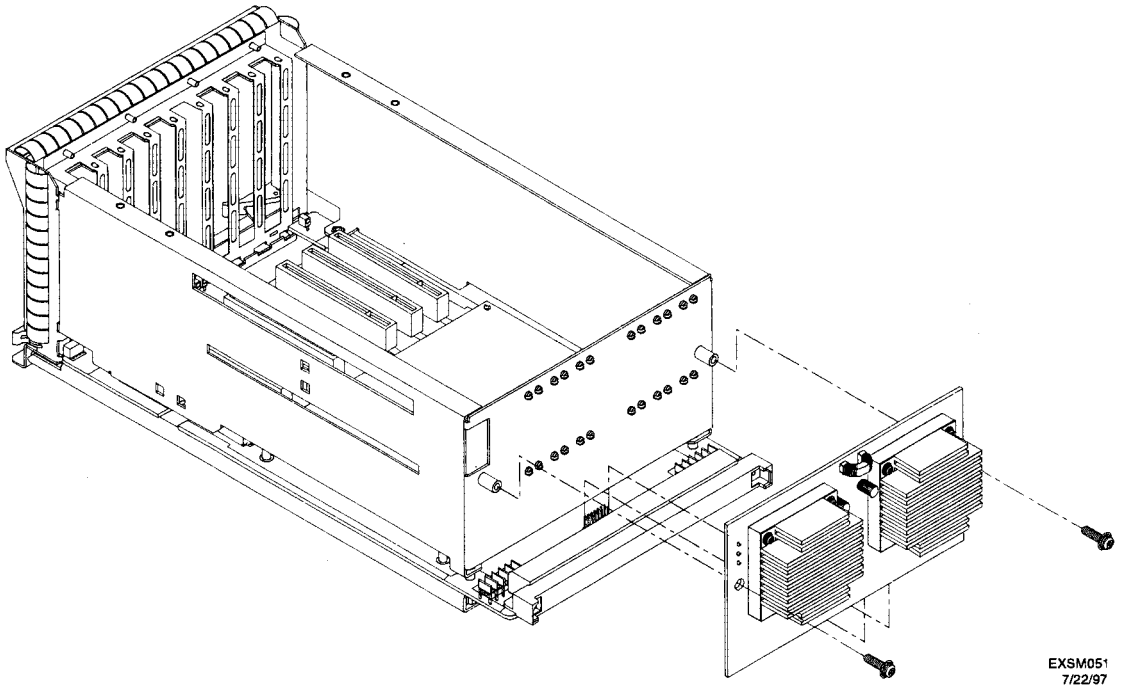
I/O board (PCI cardcage) power board

This section provides the details required to remove and install the I/O board power board.

Removal

This section provides the details required to remove the I/O board power board. Refer to Figure 26 for power board removal details.

Figure 26 I/O board power board removal



Step 1 Remove the two screws securing the power board to the rear of the chassis.

Step 2 Lift the power board up and out from the chassis.

Installation

This section provides the details required to install the I/O board power board.

Step 1 Position the power board on the rear of the chassis. Align the center connector on the rear of the power board with the pins on the I/O board.

Step 2 Press board down into position.

Step 3 Attach the power board to the chassis with two screws.

Processor board

This section provides the details required to remove and install the processor boards.

Removal

This section provides the details required to remove the processor boards.

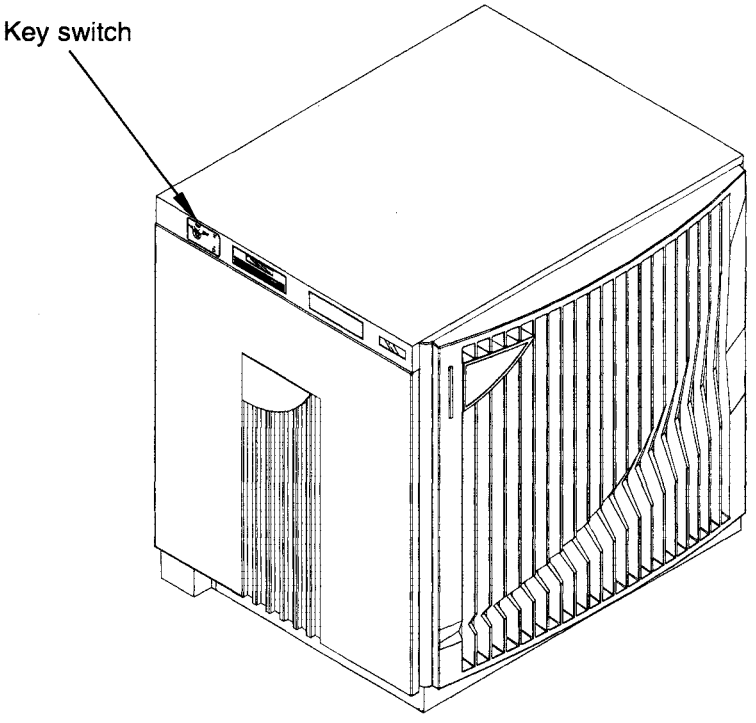
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 27 for keyswitch location.

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Figure 27 Keyswitch location

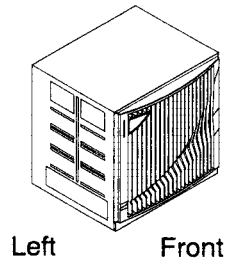


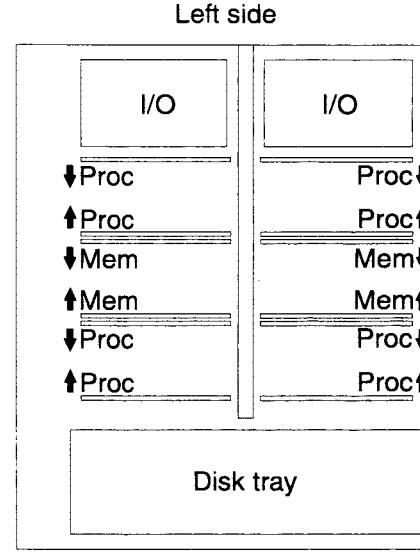
Note

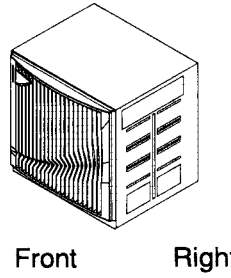
Turn off power to the system before you remove the processor card. Failure to remove power before removing the processor board will damage electronic components on the board assembly.

Step 3 Select the processor board you intend to remove. The chassis can contain as many as sixteen processor boards depending on your system configuration. The processor board you are targeting determines which side skin you need to remove. Refer to Figure 28 for locations of processor boards in the chassis. Refer to Figure 29 for locations of the processor board indicated by a specific LCD panel failure code. Refer to Figure 30 for locations of processor boards indicated by reference designator.

Figure 28 Processor board locations







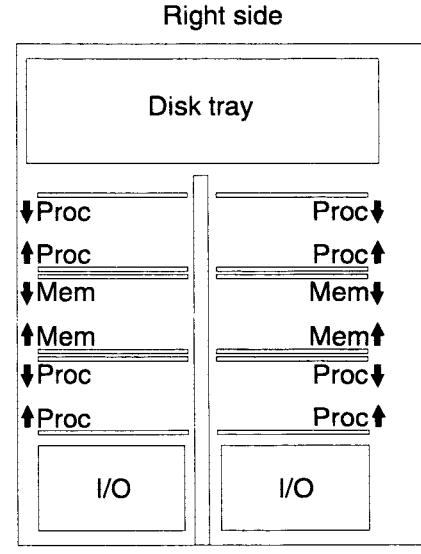


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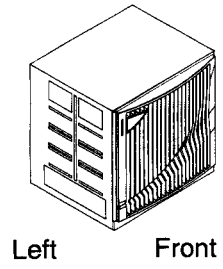
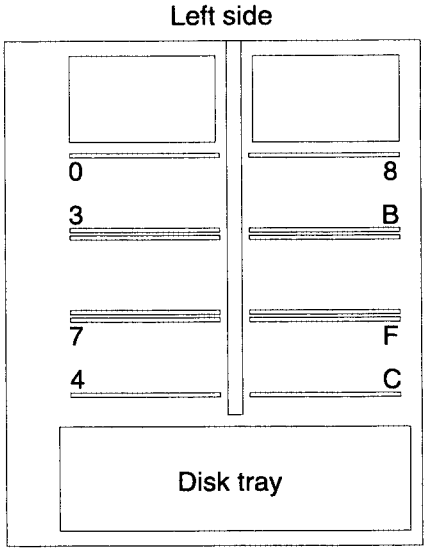
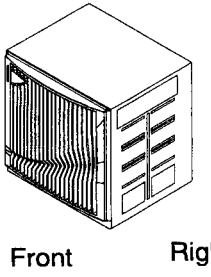
Figure 29 Processor locations by failure code







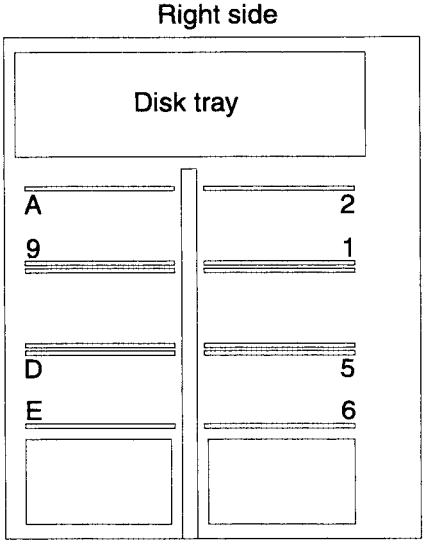


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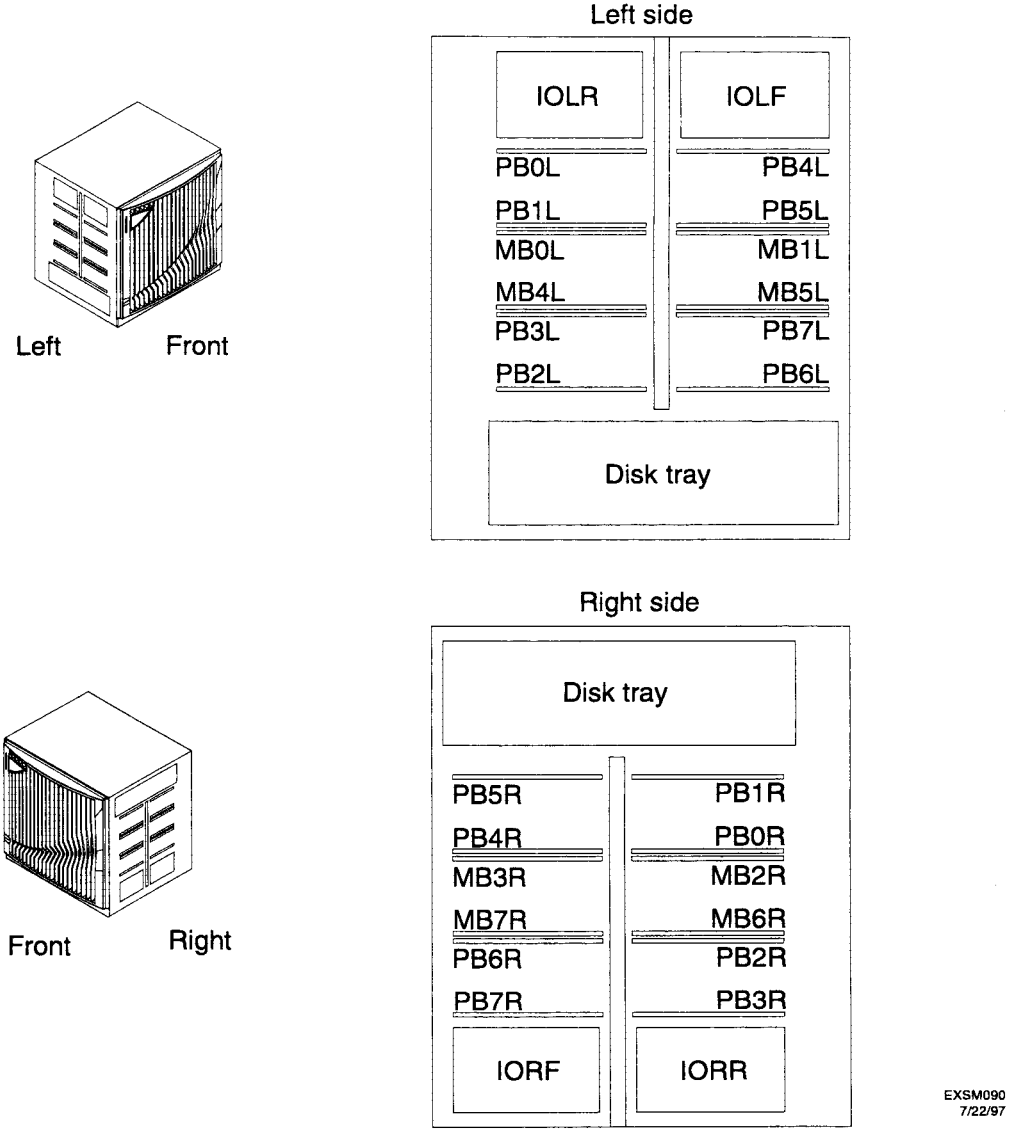
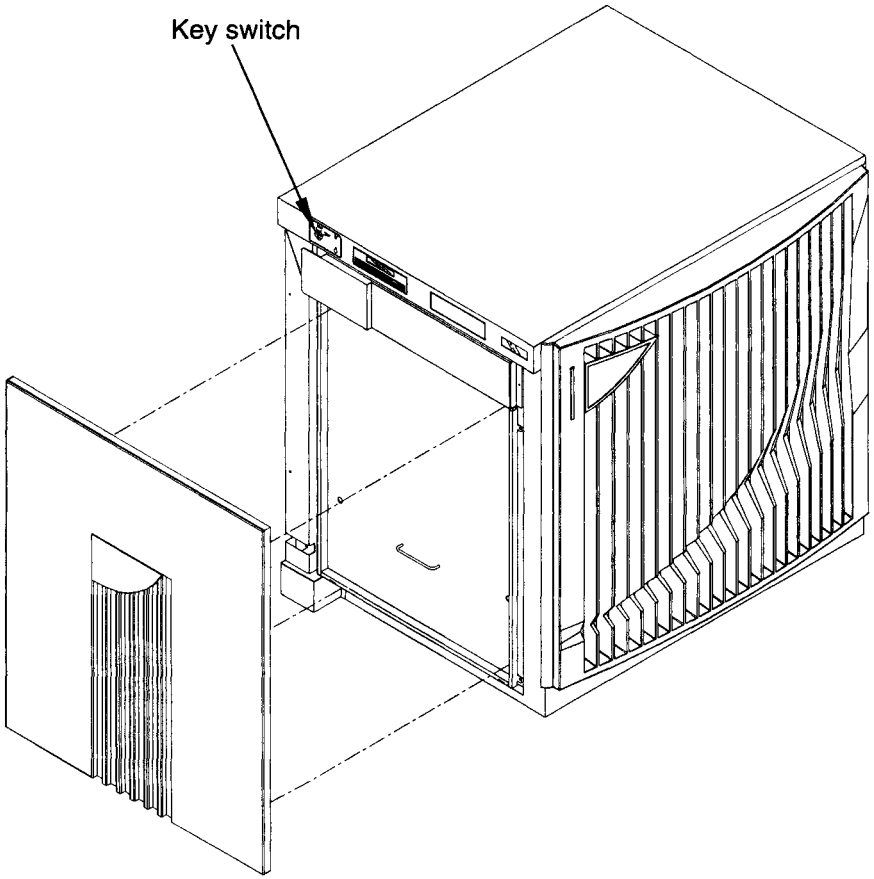
Figure 30 Processor location by reference designator



Step 4 Remove the applicable side cabinet skin by pulling from the top and bottom of the skin until it pops out. Each skin has a set of four catch pins securing it to the chassis. Refer to Figure 31 for details.

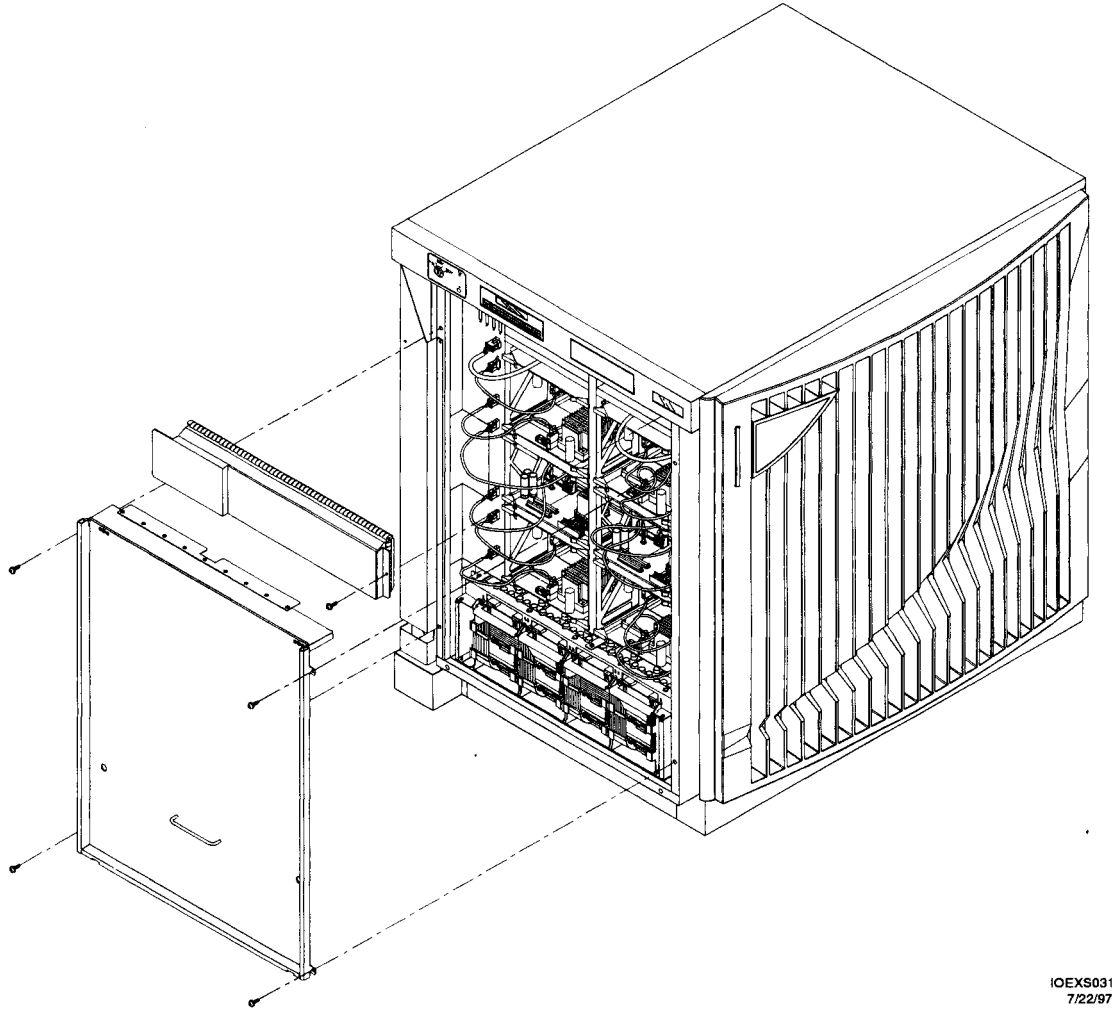
Figure 31 Side skin removal



Step 5 Remove the upper EMI panel by removing the screw that fastens the panel to the chassis. Refer to Figure 32 for details.

Step 6 Remove the lower EMI panel by removing the four screws that fasten the panel to the chassis. Refer to Figure 32 for details.

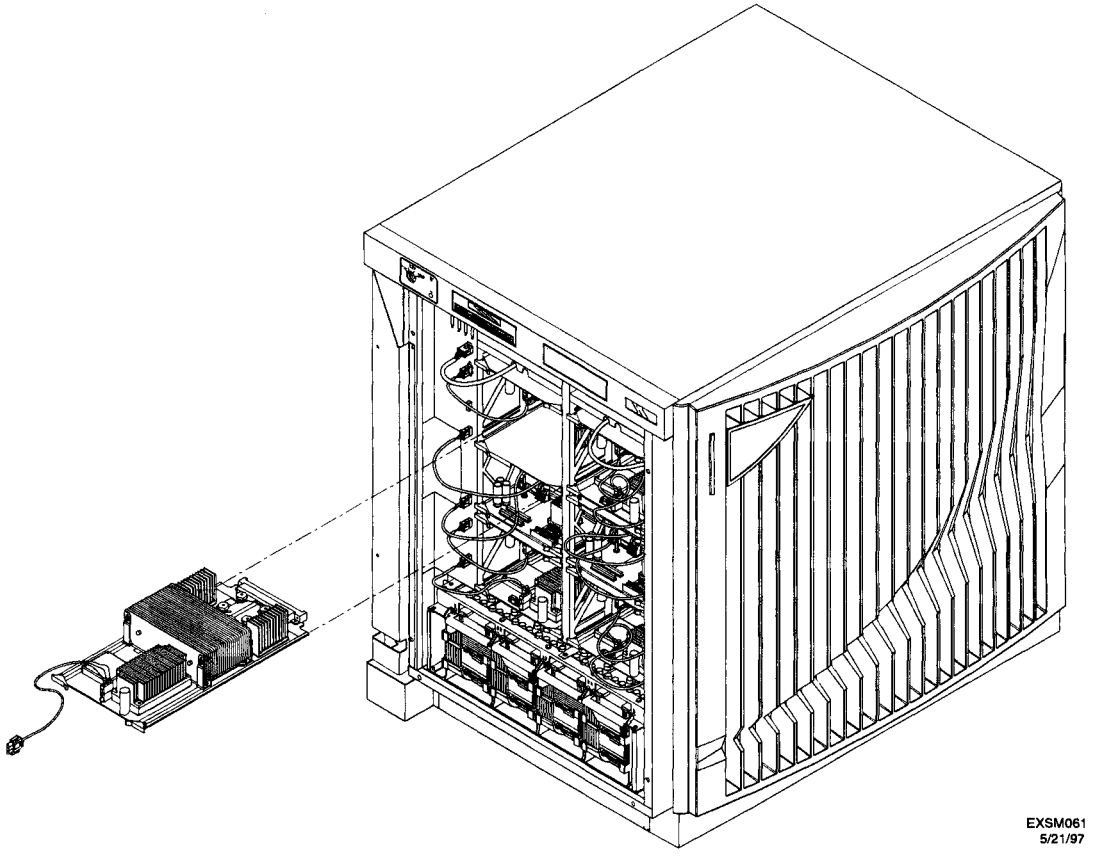
Figure 32 EMI panel removal



Step 7 Unplug the power cable for the target processor board. The power connections are labeled on the chassis. Refer to Figure 30 for reference marking details.

Step 8 Remove the processor board from the chassis by pulling the two extractor levers on the front of the processor board toward you until the processor board is unseated from the node routing board (ENRB). Continue sliding the processor board all the way out, taking care to support it underneath. Refer to Figure 33 for processor board removal details.

Figure 33 Processor board removal



Installation

This section provides the details required to install the processor board.

Step 1 Install the processor board into the chassis by lining up the processor board with the guide rails. Continue sliding the processor board into the chassis and secure it using the two extractor levers. Connect the power cable from the processor board to the chassis.

Step 2 Install the upper EMI panel. Use one screw.

Step 3 Install the lower EMI panel. Use four screws.

Step 4 Install the skin.

Memory board

This section provides the details required to remove and install the memory boards.

Removal

This section provides the details required to remove the memory boards.

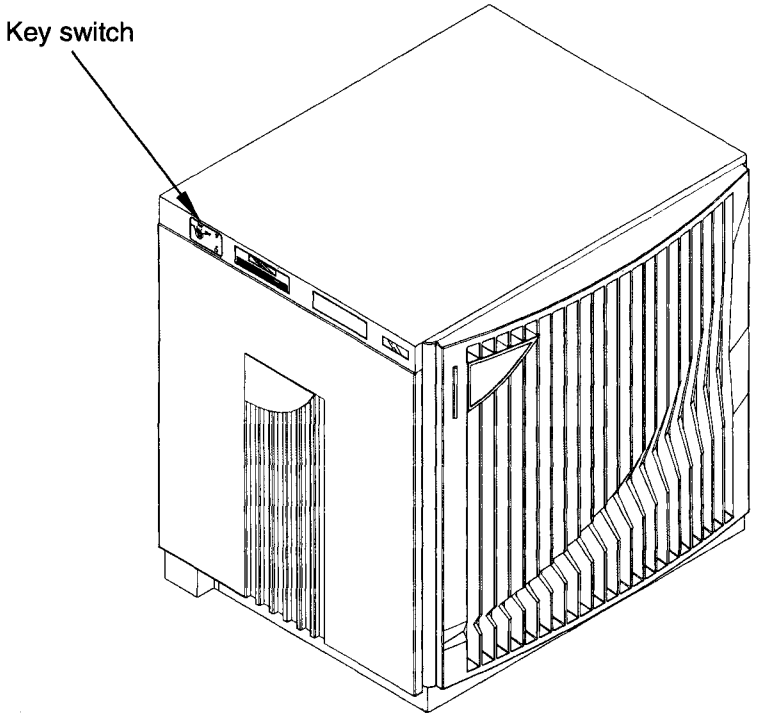
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 34 for keyswitch location.

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Figure 34 Keyswitch location



Note

Turn off power to the system before you remove the memory board. Failure to remove power before removing the memory board will damage electronic components on the board assembly.

Step 3 Select the memory board you intend to remove. The chassis can contain as many as eight memory boards depending on your system configuration. The memory board you are targeting determines which side skin you need to remove. Figure 35 shows the possible locations of memory boards in the chassis. Figure 36 shows the locations of memory boards indicated by reference designator.

Figure 35 Memory board locations

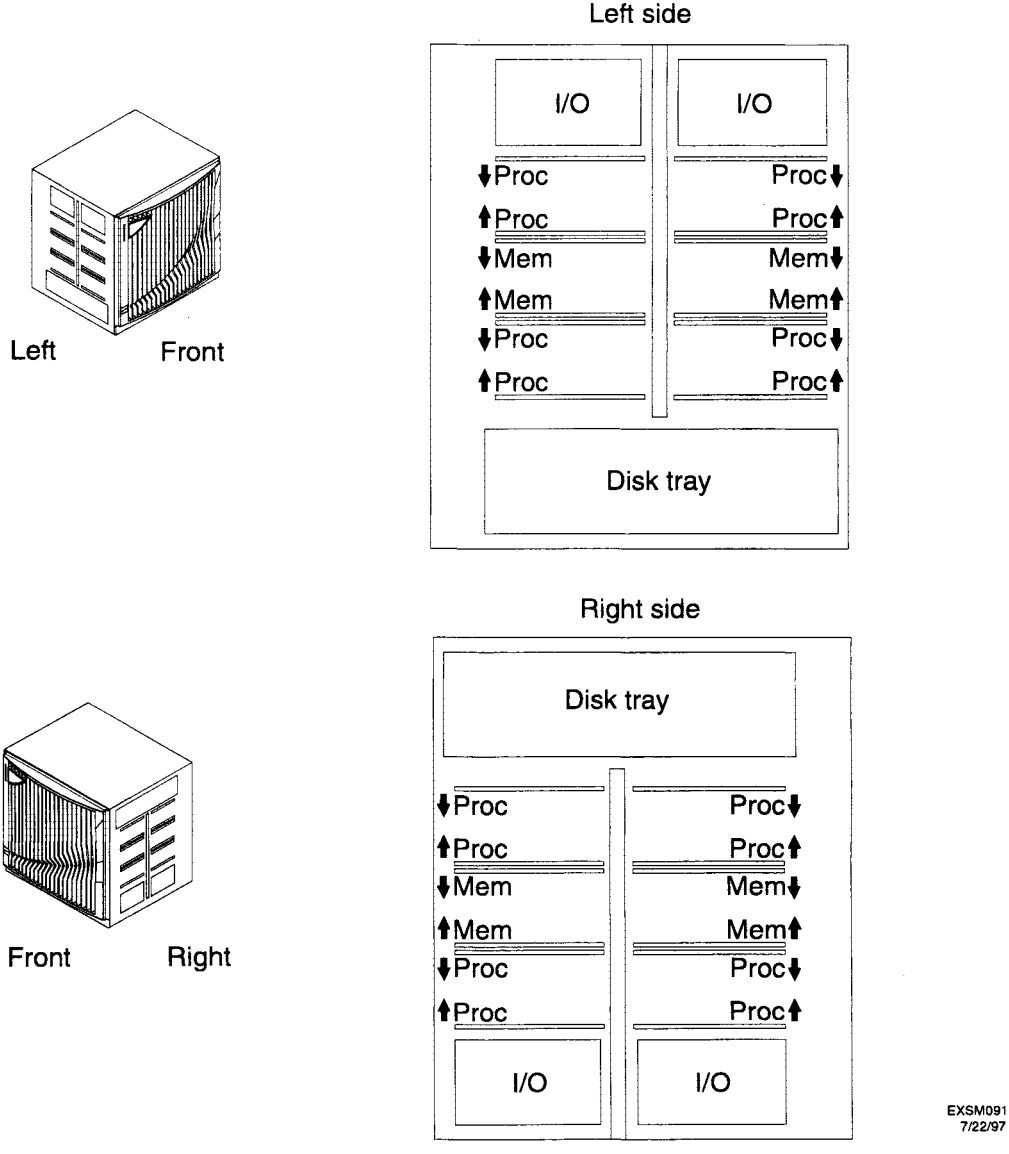
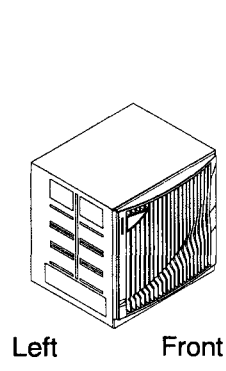
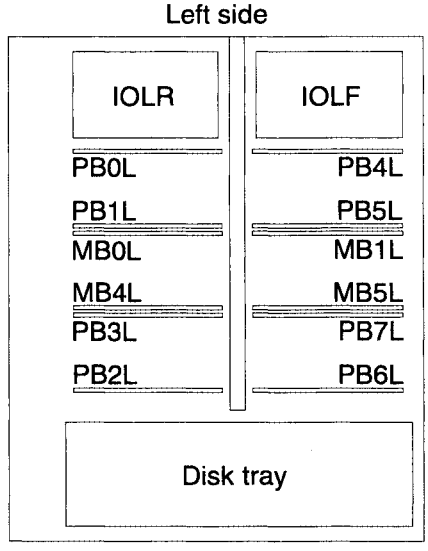
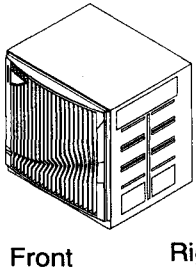
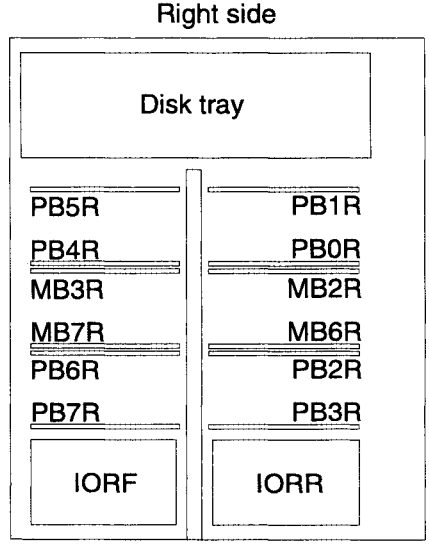


Figure 36 Memory location by reference designator









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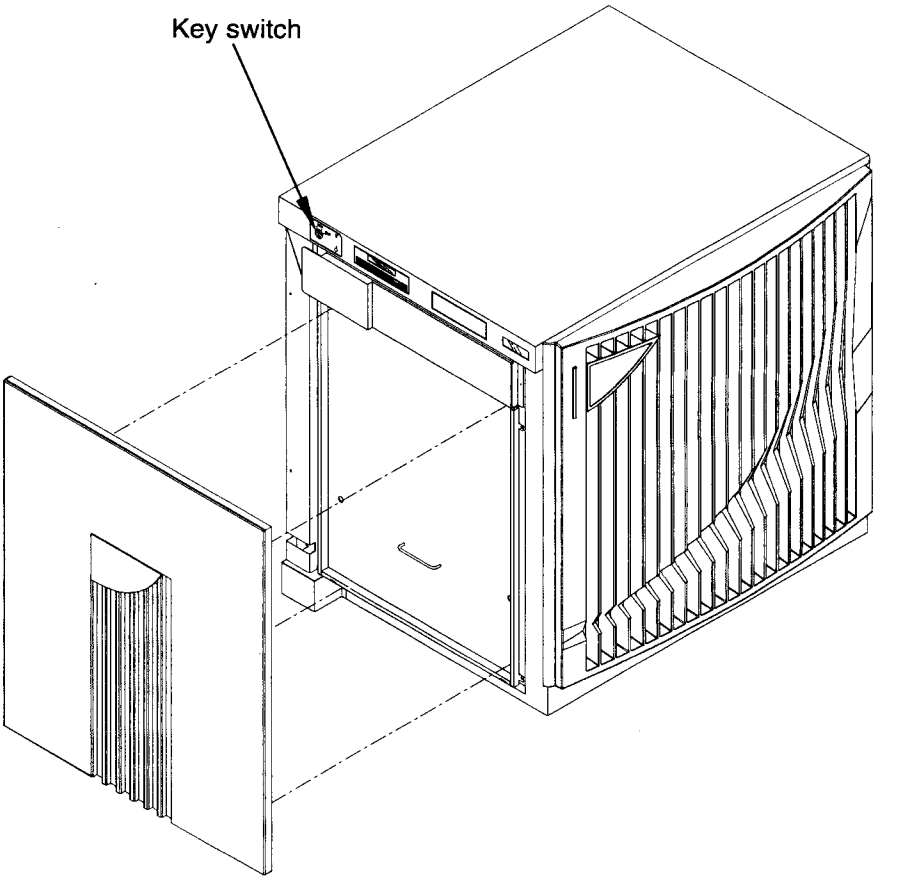
Step 4 Remove the applicable side cabinet skin by pulling from the top and bottom of the skin until it pops out. Each skin has a set of four catch pins securing it to the chassis. Refer to Figure 37 for details.

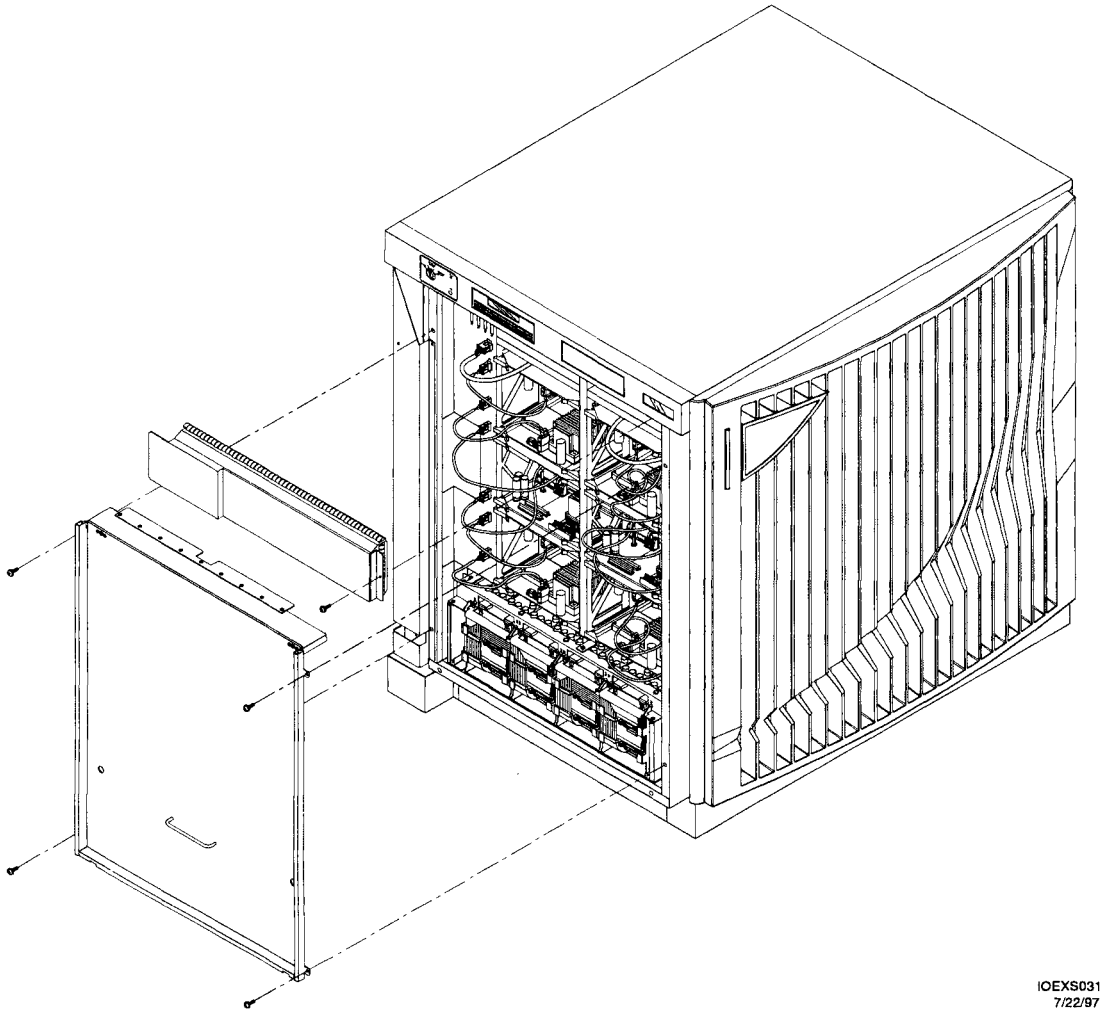
Figure 37 Side skin removal



Step 5 Remove the upper EMI panel by removing the screw that fastens the panel to the chassis. Refer to Figure 38 for details.

Step 6 Remove the lower EMI panel by removing the four screws that fasten the panel to the chassis. Refer to Figure 38 for details.

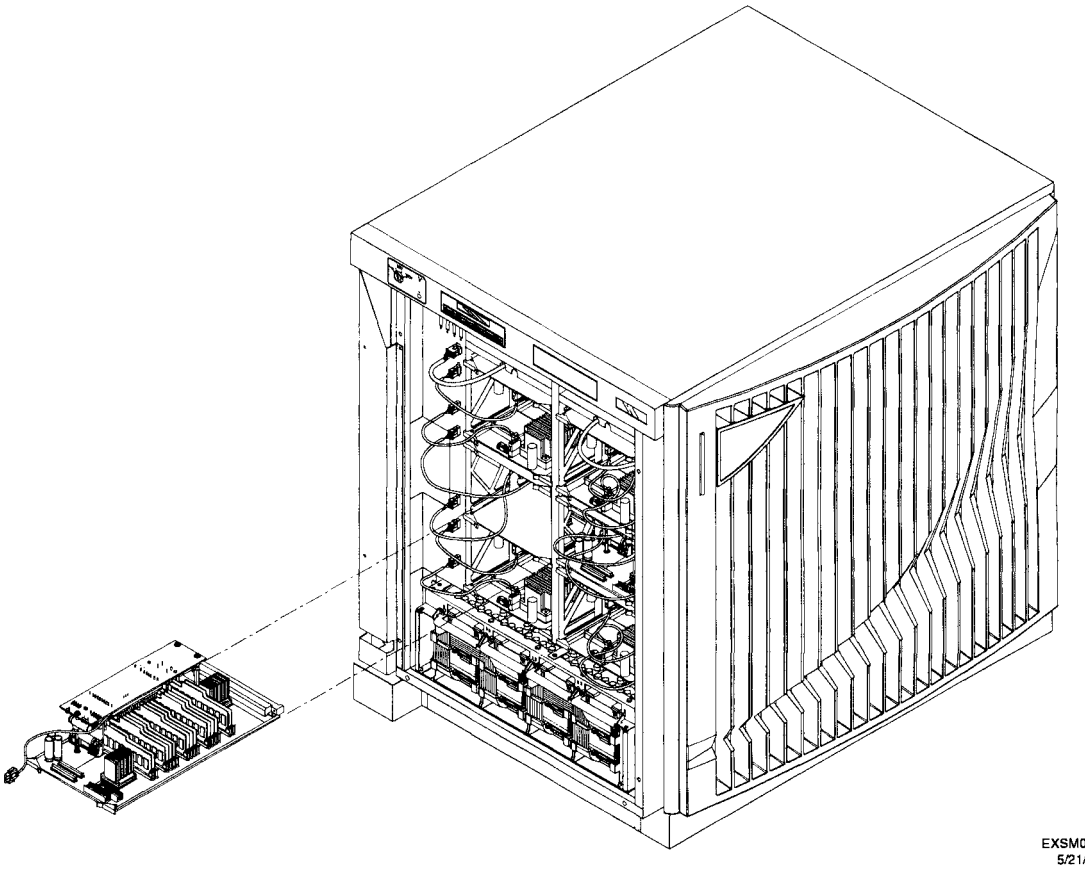
Figure 38 EMI panel removal



Step 7 Unplug the power cable for the target memory board. The power connections are labeled on the chassis. Refer to Figure 36 for reference marking details.

Step 8 Remove the memory board from the chassis by pulling the two extractor levers on the front of the memory board toward you until the memory board is unseated from the node routing board (ENRB). Continue sliding the memory board all the way out, taking care to support it underneath. Refer to Figure 39 for memory board removal details.

Figure 39 Memory board removal



Installation

This section provides the details required to install the memory board.

Step 1 Install the memory board into the chassis by lining up the memory board with the guide rails. Continue sliding the memory board into the chassis and secure it using the two extractor levers. Connect the power cable from the memory board to the chassis.

Step 2 Install the lower EMI panel. Use four screws.

Step 3 Install the upper EMI panel. Use one screw.

Step 4 Install the skin.

Memory board power board

This section provides the details required to remove and install the memory board power board.

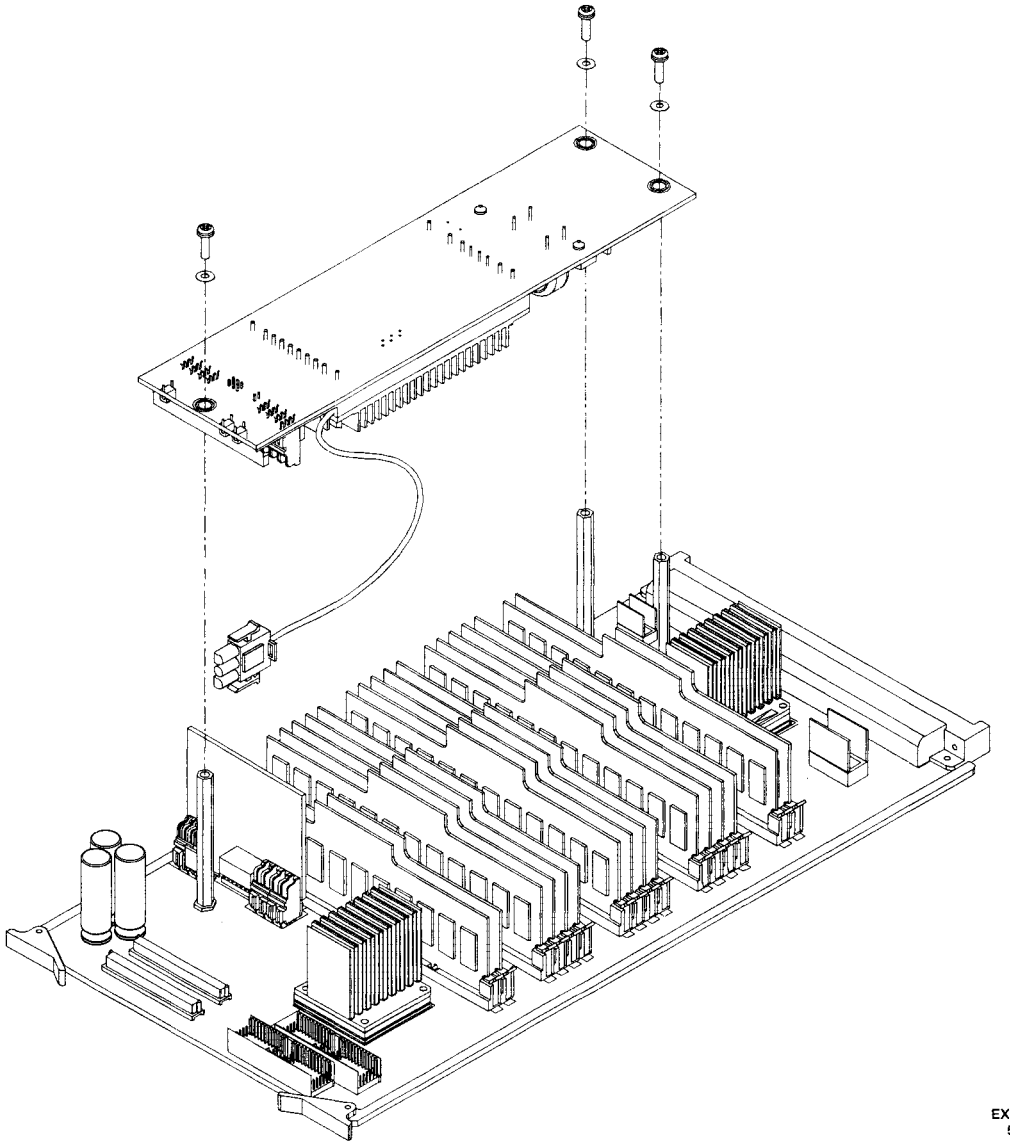
Removal

This section provides the details required to remove the memory board power board. Refer to Figure 40 for details.

Step 1 Remove three screws attaching the memory board power board to the standoffs.

Step 2 Gently lift power board, unplugging it from the interconnect board.

Figure 40 Memory board power board replacement



Installation

This section provides the details required to install the memory board power board.

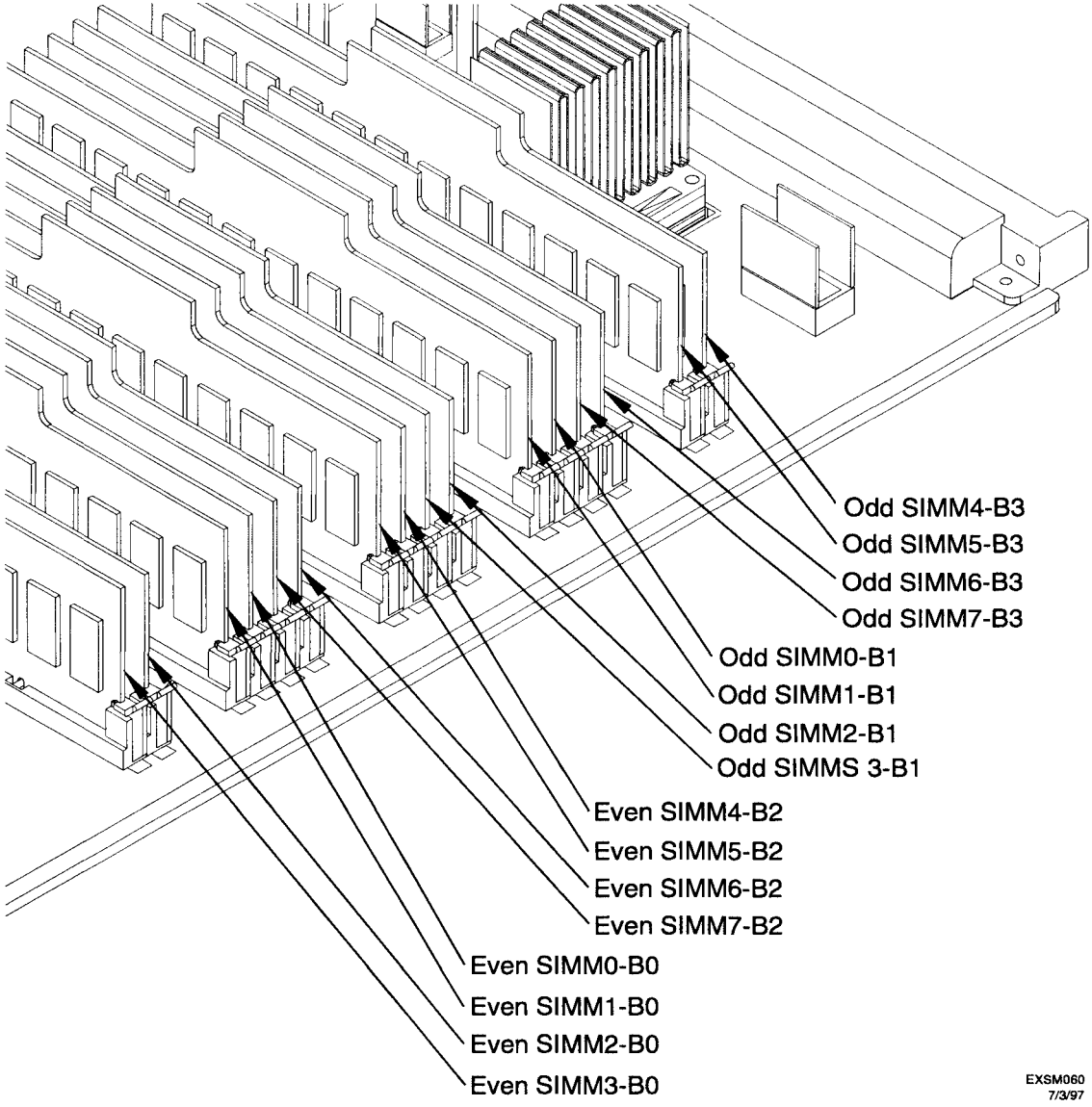
Step 1 Position power board above the three standoffs and connect to interconnect board.

Step 2 Install three screws to attach the memory board power board to the standoffs.

Plug-in memory boards

This section provides the details required to remove and install the plug-in memory boards. Refer to Figure 41 for SIMM designators.

Figure 41 SIMM designators



Removal

This section provides the details required to remove the plug-in memory boards. Refer to Figure 41 for plug-in memory board details.

Step 1 Remove memory board power board from the memory board.

Step 2 Depress the tabs on each end of the plug-in memory board socket.

Step 3 Remove the plug-in memory board.

Installation

This section provides the details required to install the plug-in memory boards.

Step 1 Depress the tabs on each end of the plug-in memory board socket.

Step 2 Install the plug-in memory board.

Step 3 Install memory board power board on the memory board.

Disk tray

The following sections provide the information required to remove and install the disk tray.

Removal

This section provides the details required to remove the disk tray.

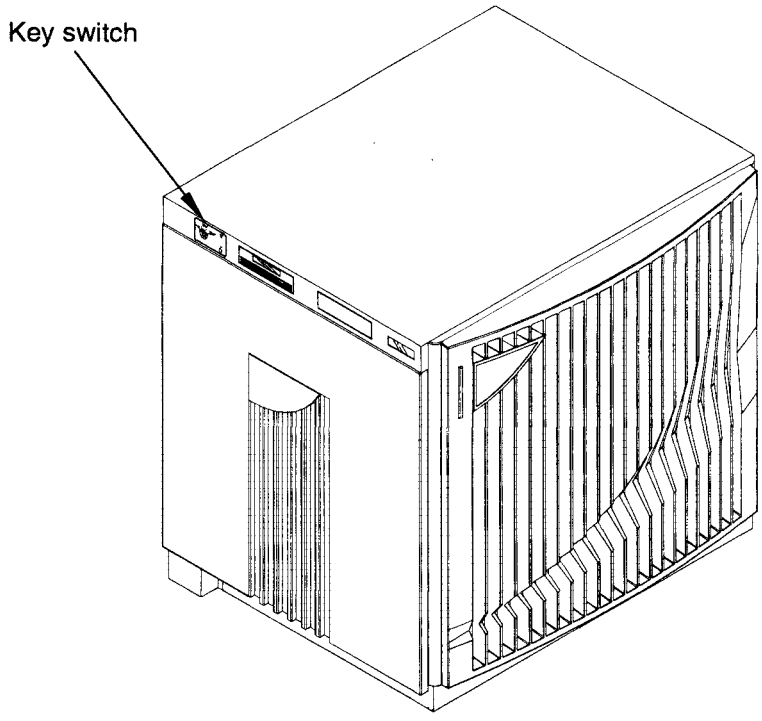
Step 1 Shut down the system with the `/etc/shutdown` command.

`/etc/shutdown -h` *time*

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 42 for keyswitch location.

Figure 42 Keyswitch location

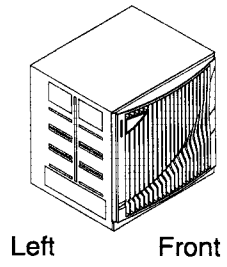


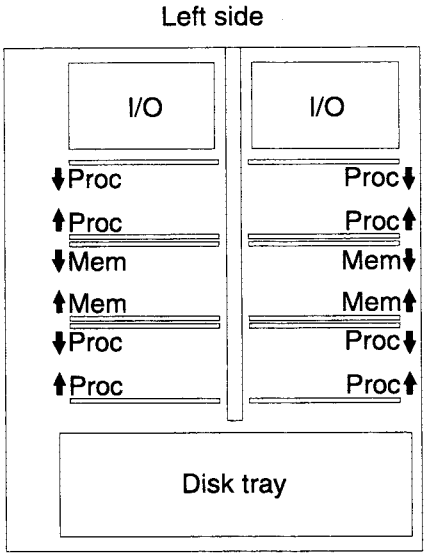
Note

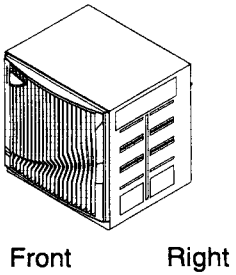
Turn off power to the system before you remove the PCI cardcage. Failure to remove power before removing the PCI cardcage will damage electronic components on the board assembly.

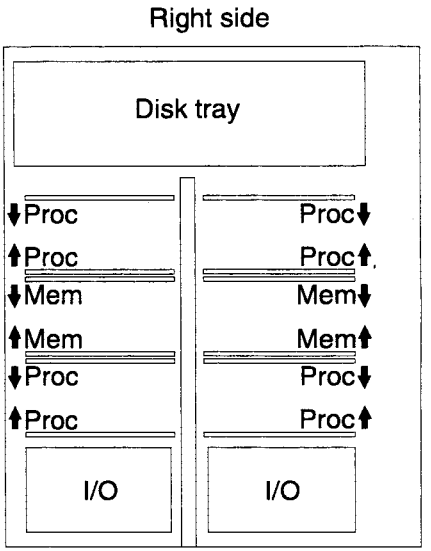
Step 3 Select the disk tray you intend to remove. The chassis can contain one or two disk trays, depending on your system configuration. The disk tray you are targeting determines which side skin you need to remove. Figure 43 shows the possible locations of disk trays in the chassis.

Figure 43 Disk tray locations









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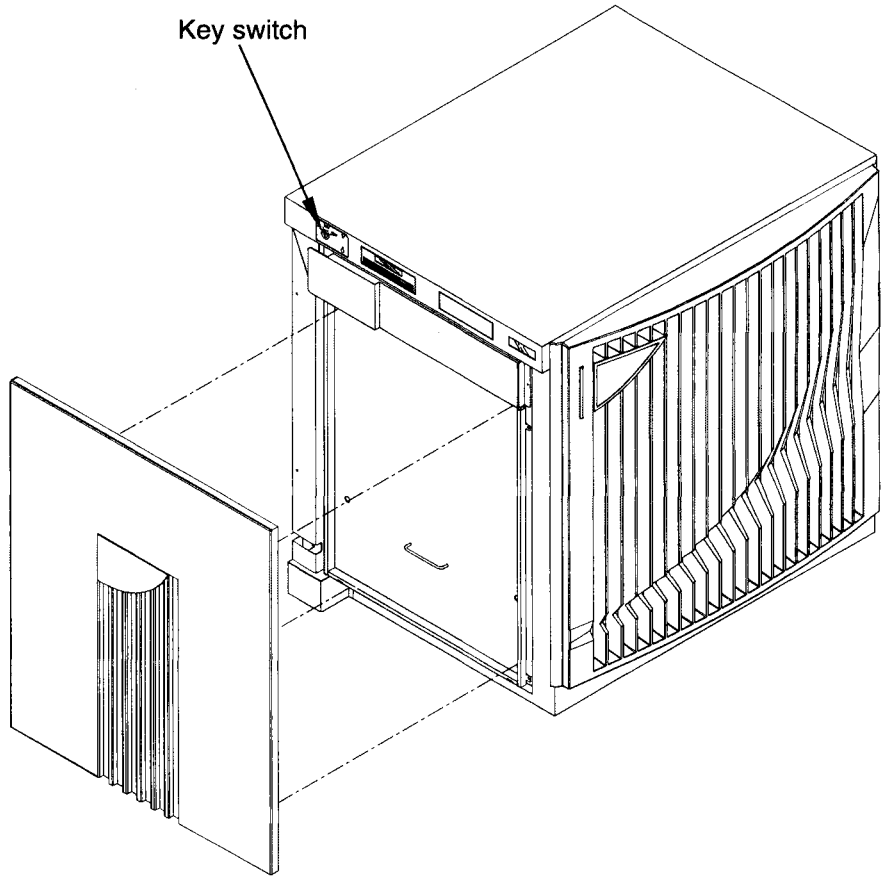
Step 4 Remove the left side cabinet skin by pulling from the top and bottom of the skin until it pops out. The skin has a set of four catch pins that secure it to the chassis. Refer to Figure 44 for skin removal details.

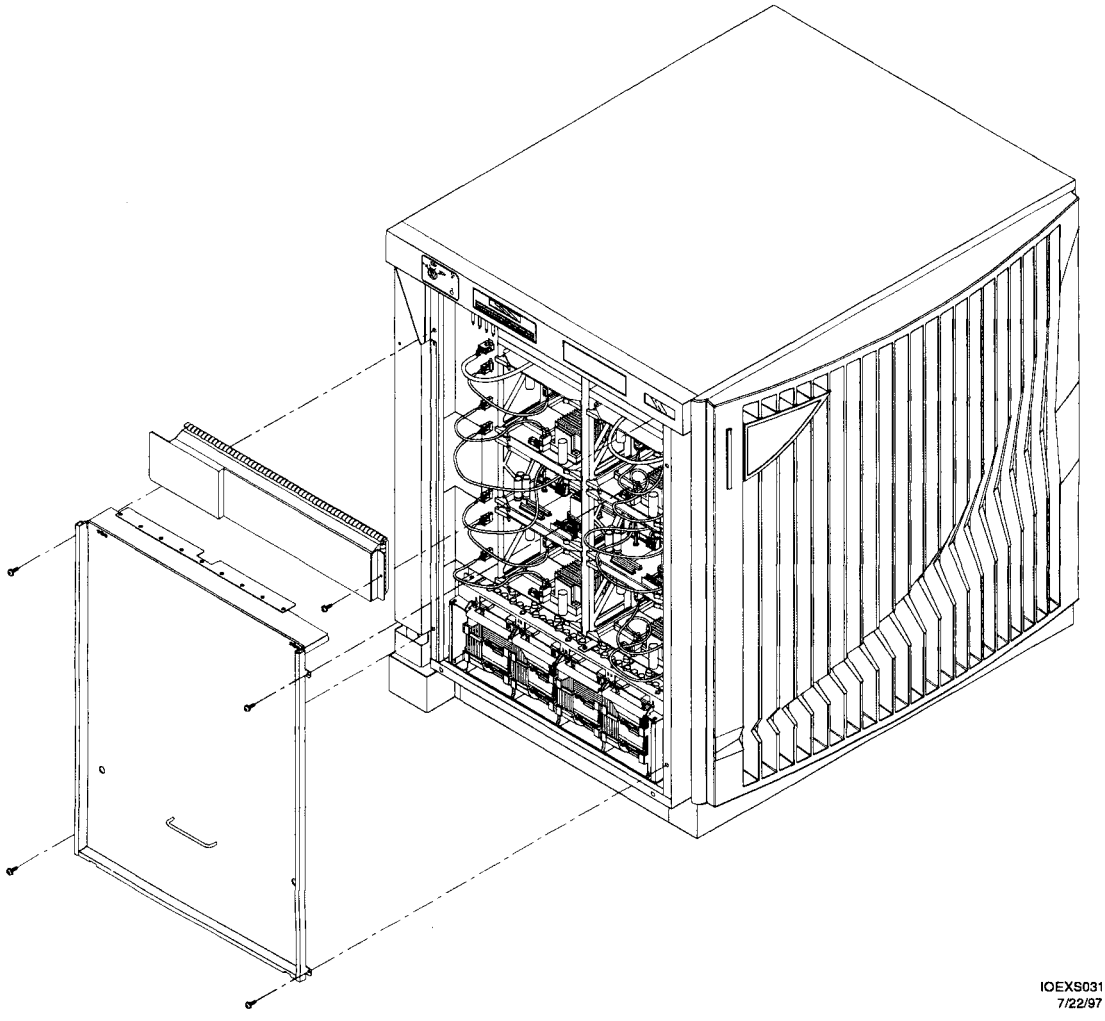
Figure 44 Side cabinet skin removal



Step 5 Remove the upper EMI panel by removing the one screw on the sids of the panel. Refer to Figure 45 for panel removal details.

Step 6 Remove the lower EMI panel by removing four screws on the sides of the panel. Refer to Figure 45 for panel removal details.

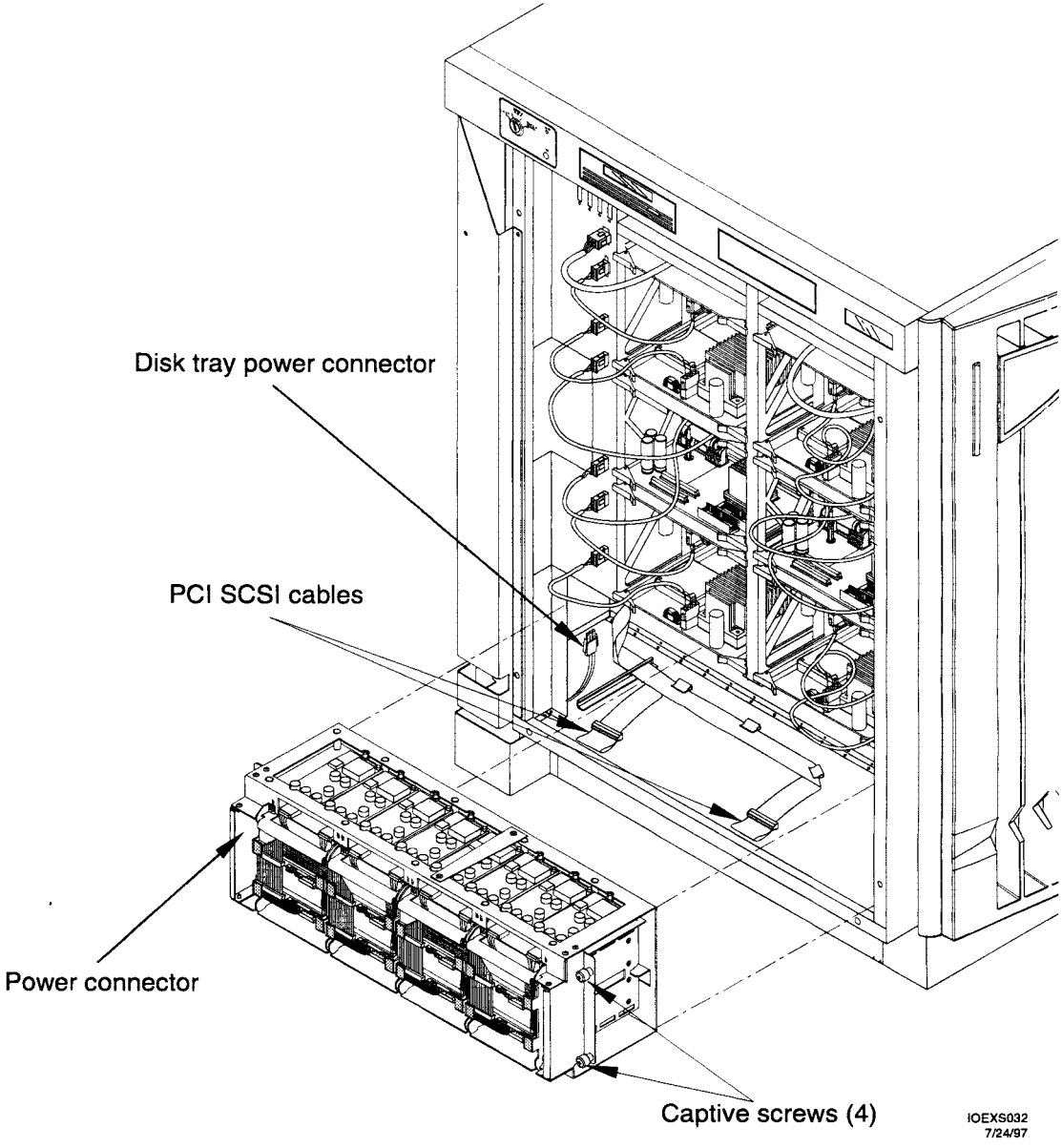
Figure 45 EMI panel removal



Step 7 Locate the disk tray on the bottom left side of the chassis.

Step 8 Disconnect the power cable from the disk tray. It is located on the left side of the disk tray and is visible by looking straight into the left side of the disk tray. Refer to Figure 46 for disk tray removal details.

Figure 46 Disk tray removal



Step 9 Loosen the two captive screws on both sides of the disk tray.

Step 10 Remove the disk tray only enough to disconnect the PCI SCSI cables from the disk tray. Use only the cable connector clips to remove the SCSI connectors to prevent damage to the cables.

Step 11 Slide the disk tray out of the chassis.

Installation

This section provides the details required to install the disk tray.

Step 1 Slide the disk tray partially into the chassis.

Step 2 Connect the SCSI cables from the chassis to the disk tray.

Step 3 Connect the power cord to the disk tray.

Step 4 Slide the disk tray fully into the chassis. If the disk tray does not slide freely, ensure that cables behind the tray are not presenting interference.

Step 5 Tighten the four captive screws.

Step 6 Install the lower EMI panel. Use four screws.

Step 7 Install the upper EMI panel. Use one screw.

Step 8 Install the skin.

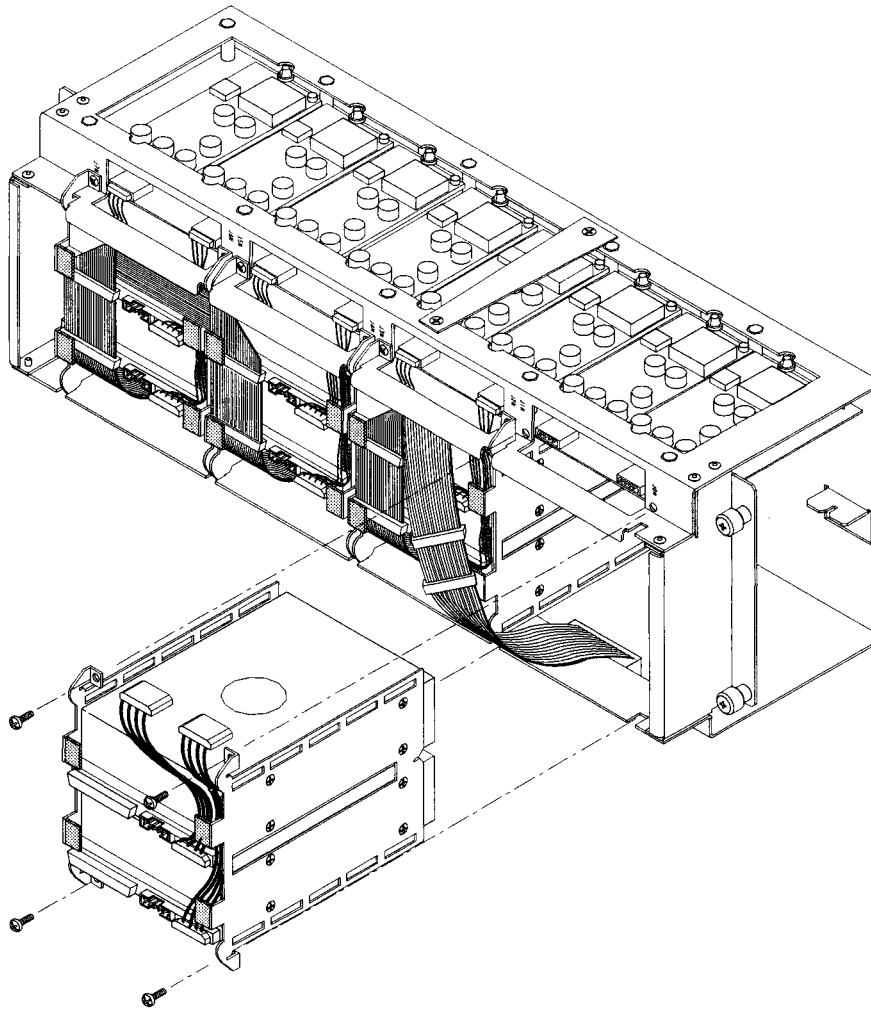
Disk pair

The following sections provide the information required to remove and install a disk pair.

Removal

This section provides the details required to remove the disk tray. Refer to Figure 47 for disk pair removal details.

Figure 47 Disk pair removal



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Step 1 Disconnect the disk dc power cables.

Step 2 Disconnect the SCSI cables from disk pair assembly. Use only the cable connector clips to remove the SCSI connectors to prevent damage to the cables.

Step 3 Remove the two screws on the top and the two screws on the bottom of the disk pair assembly.

Step 4 Slide the disk pair from the disk tray.

Installation

This section provides the details required to install the disk pair.

Step 1 Position the disk pair in the disk tray.

Step 2 Attach the disk pair to the disk tray by installing four screws.

Step 3 Connect the dc power cables to each disk.

Step 4 Connect the SCSI cables to each disk.

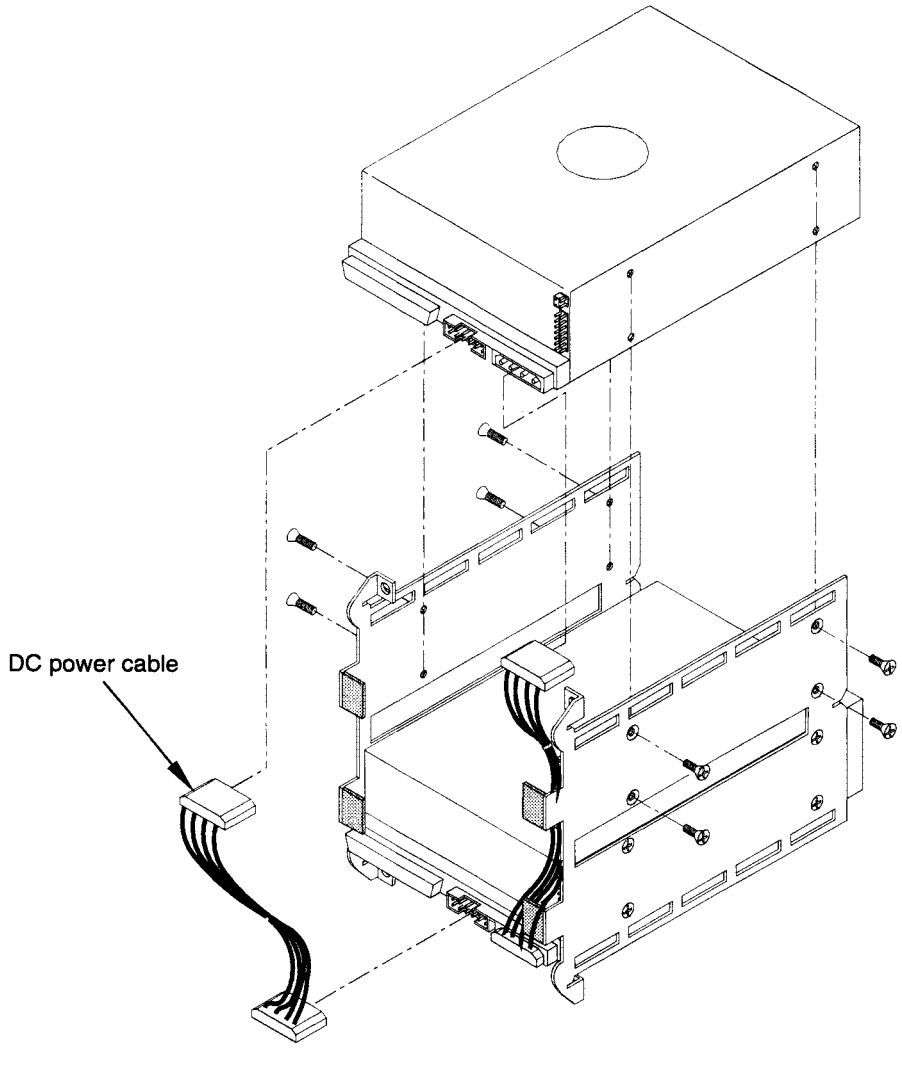
Single disk

The following sections provide the information required to remove and install a single disk.

Removal

This section provides the details required to remove a disk from the disk pair assembly. Refer to Figure 48 for single disk removal details.

Figure 48 Single disk removal



Step 1 Remove four screws from each side of the mounting bracket.

Step 2 Remove the disk drive from the disk pair assembly.

Step 3 Remove the dc power connector from the drive that is being replaced.

Installation

This section provides the details required to install a disk in a disk pair assembly.

Step 1 Connect the dc power cable removed from the disk being replaced.

Step 2 Position the disk in the disk pair assembly.

Step 3 Attach the disk to the disk pair assembly by installing four screws on each side of the assembly.

Disk tray power module

The following sections provide the information required to remove and install a disk tray power module.

Removal

This section provides the details required to remove a dc power module from the disk tray assembly. Refer to Figure 49 for power module removal details.

Step 1 Loosen the two lockdowns securing the power module in place. Turn lockdowns counterclockwise until they clear the power module.

Step 2 Lift the power module from the disk tray.

Installation

This section provides the details required to install a dc power module in a disk tray assembly.

Note

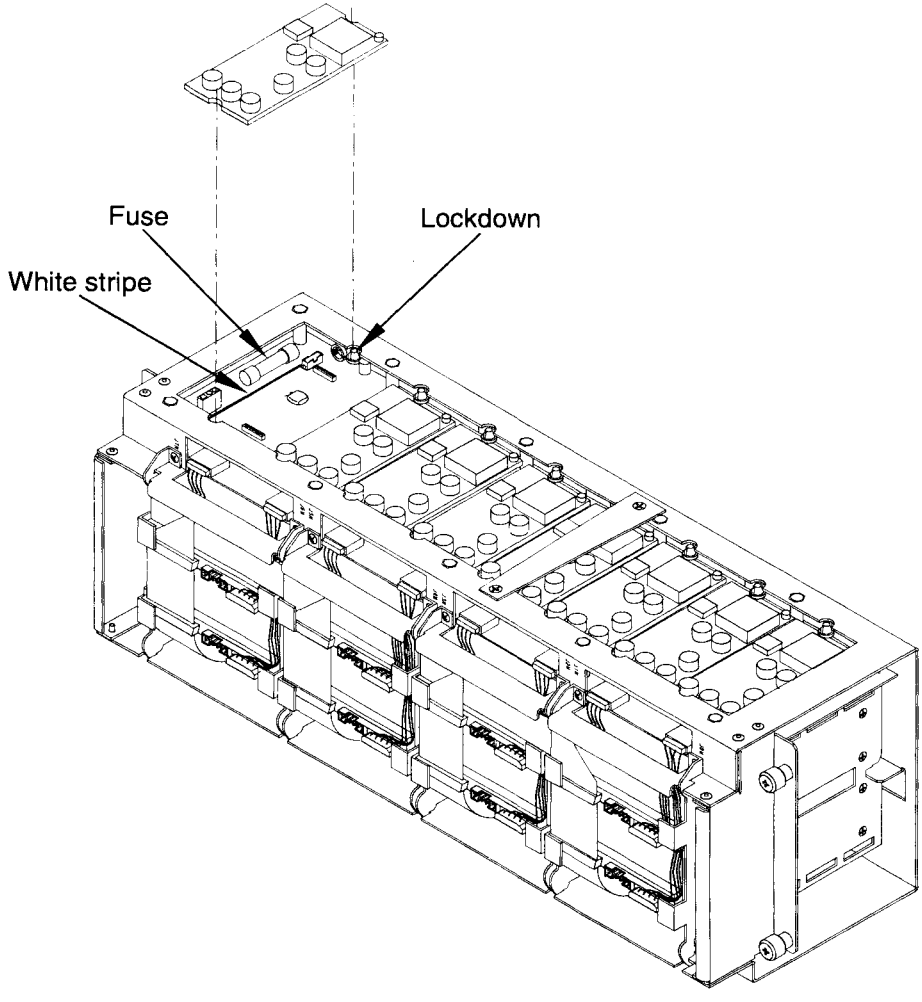
Position the dc power module so the large capacitors on the edge of the module are positioned toward the connectors on the disk tray power board.

Step 1 Replace the fuse associated with the power board being replaced.

Step 2 Position the module in the disk tray. Ensure that the edge of the module is immediately adjacent to the white line on the disk tray.

Step 3 Rotate the two lockdowns to secure the module in place.

Figure 49 Disk tray power module removal



DAT drive

The following sections provide the information required to remove and install a DAT drive.

Removal

This section provides the details required to remove a DAT drive assembly.

Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 50 for keyswitch location.

Step 3 Set the AC input circuit breaker to **OFF**.

Figure 50 Keyswitch location

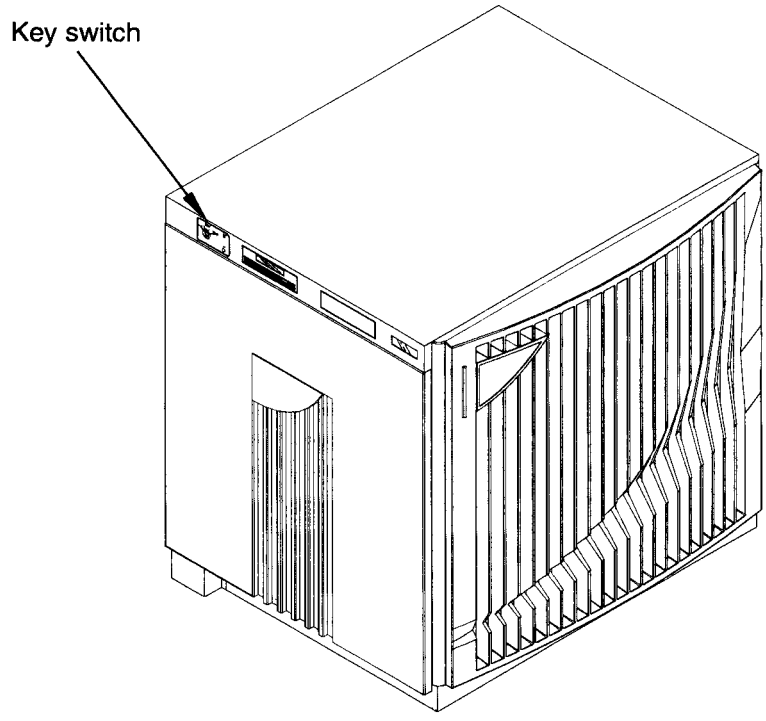


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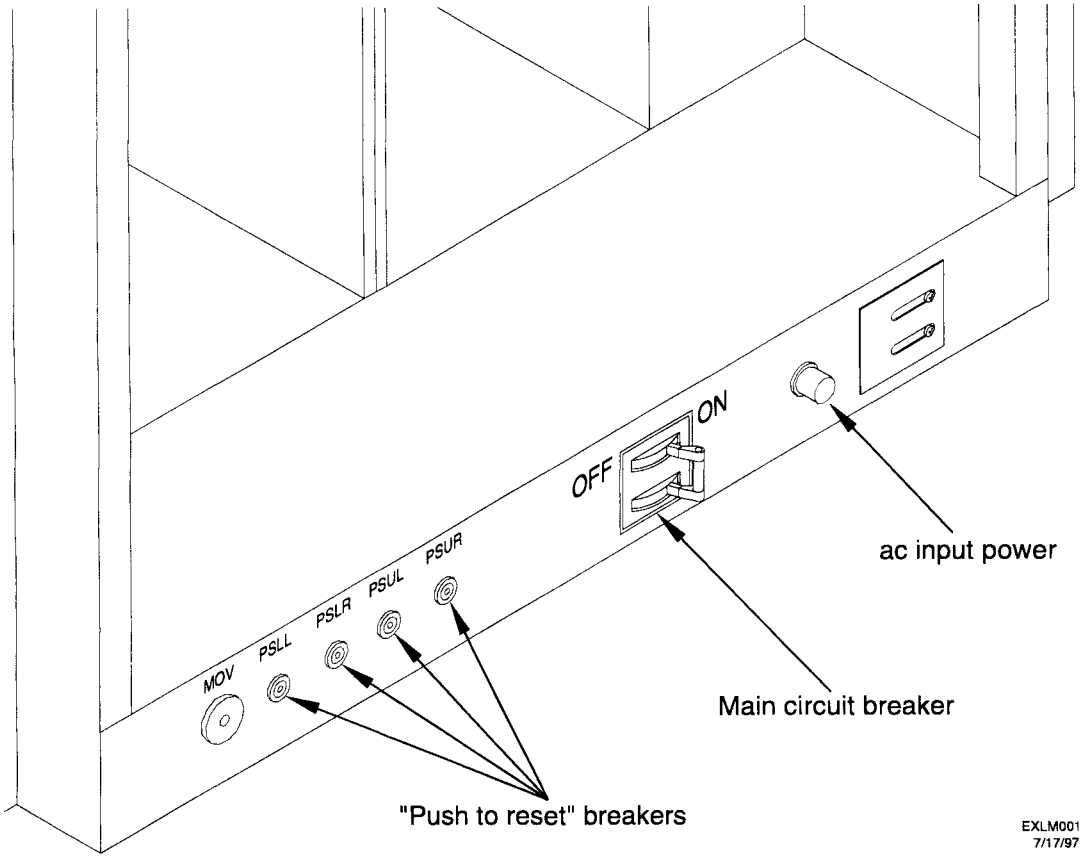
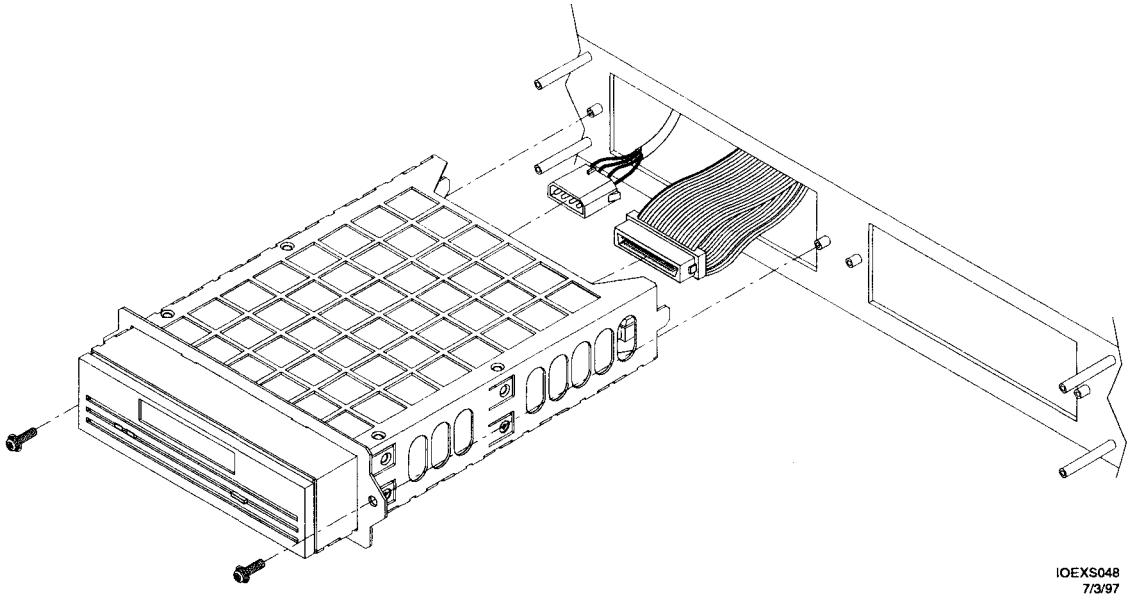
Figure 51 Inpuit circuit breaker location



Step 4 Remove the LCD control panel by removing four screws securing the panel. Carefully place the LCD control panel on top of the chassis.

Step 5 Remove the two screws securing the DAT drive assembly. Refer to Figure 52 for details.

Figure 52 DAT drive removal



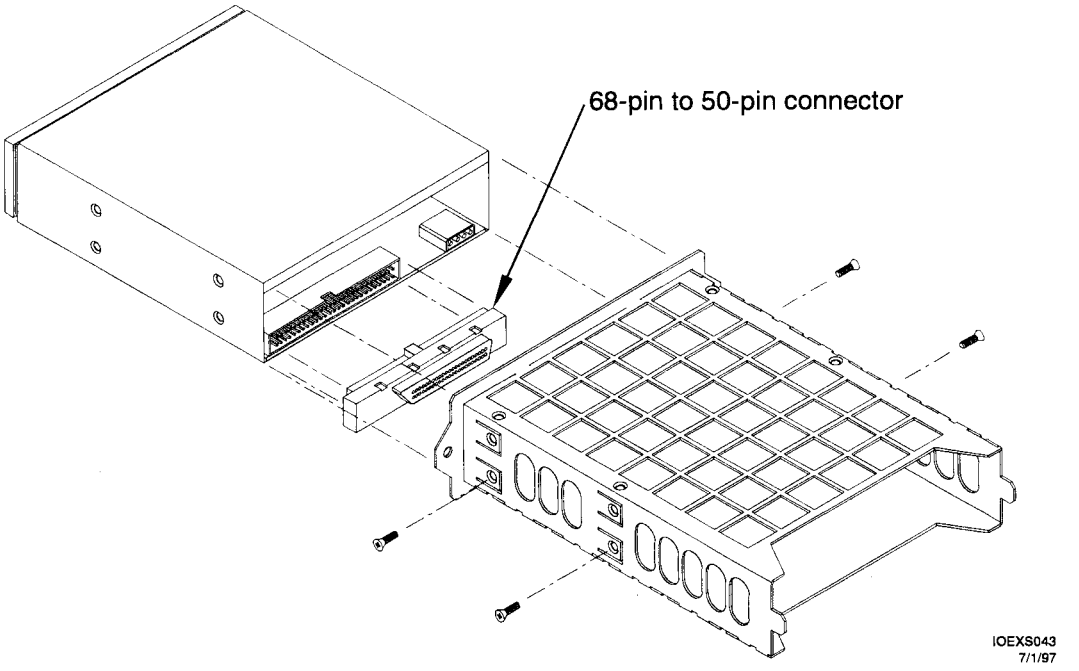
Step 6 Slide the DAT drive assembly from the DAT drive bay.

Step 7 Disconnect the SCSI cable from the rear of the DAT drive assembly.

Step 8 Disconnect the power cable from the rear of the DAT drive assembly.

Step 9 Remove the DAT drive from the drive cage by removing four screws (two on either side) and sliding the DAT drive out of the drive cage. Refer to Figure 53 for details.

Figure 53 DAT drive cage removal



Step 10 Remove the 68-pin to 50-pin adapter from the SCSI connector of the DDS-2 DAT drive. Retain the adapter for later use.

Installation

This section provides the details required to install a DAT drive assembly.

Step 1 Install the 68-pin to 50-pin adapter taken from the old drive onto the SCSI connector of the replacement DDS-2 DAT drive. Refer to Figure 53 for details.

Step 2 Verify that the jumpers are set correctly. Check that the settings are the same as those on the removed drive.

Step 3 Insert the new DAT drive into the drive cage and secure it with four screws.

Step 4 Attach the SCSI cable to the back of the DAT drive.

Step 5 Attach the power cable to the back of the DAT drive.

Step 6 Slide the DAT drive cage assembly into the drive bay. The SCSI cable and power supply cable should fold up and over the top of the drive and lay flat.

Step 7 Mate the tabs on each side of the DAT drive cage assembly with the corresponding slots in the back wall of the drive bay.

Step 8 Secure the DAT drive cage assembly with two screws.

Step 9 Install the LCD control panel using four screws.

Node routing board(ENRB)

The following sections provide the information required to remove and install the node routing board.

Removal

This section provides the details required to remove the node routing board.

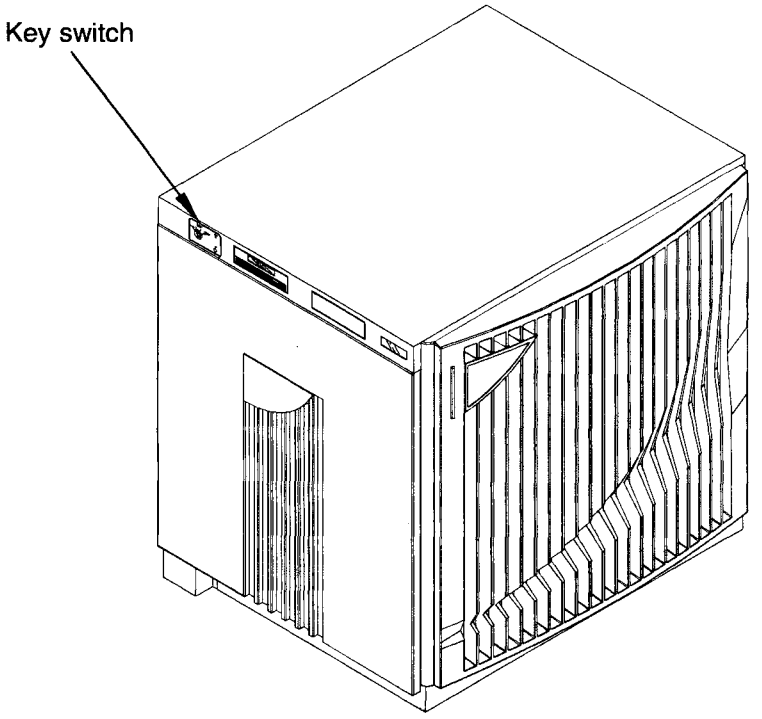
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 54 for keyswitch location.

Figure 54 Keyswitch location

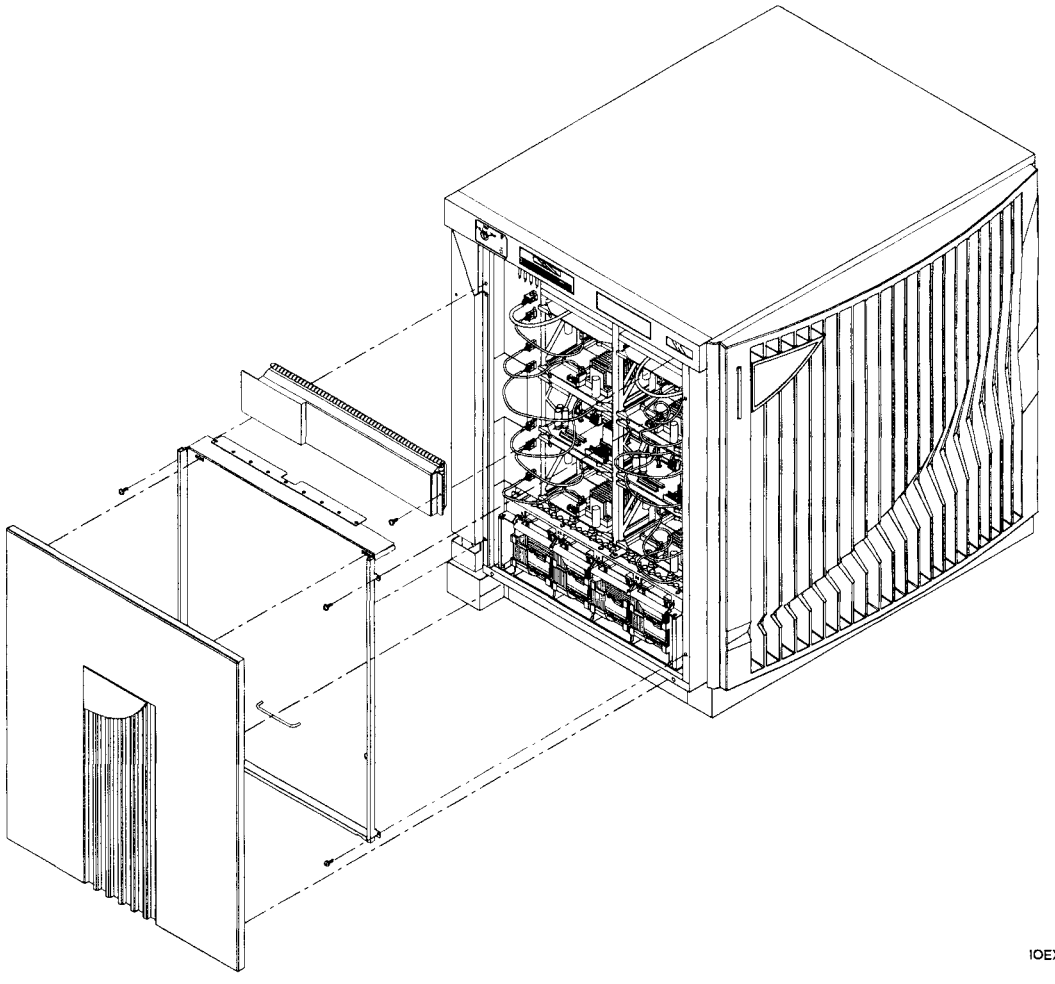


Note

Turn off power to the system before you remove the node routing board. Failure to remove power before removing the node routing board will damage electronic components on the board assembly.

Step 3 Remove both side cabinet skins by pulling from the top and bottom of the skin until it pops out. Each skin has a set of four catch pins securing it to the chassis as shown in Figure 55.

Figure 55 Side skin and EMI cover removal

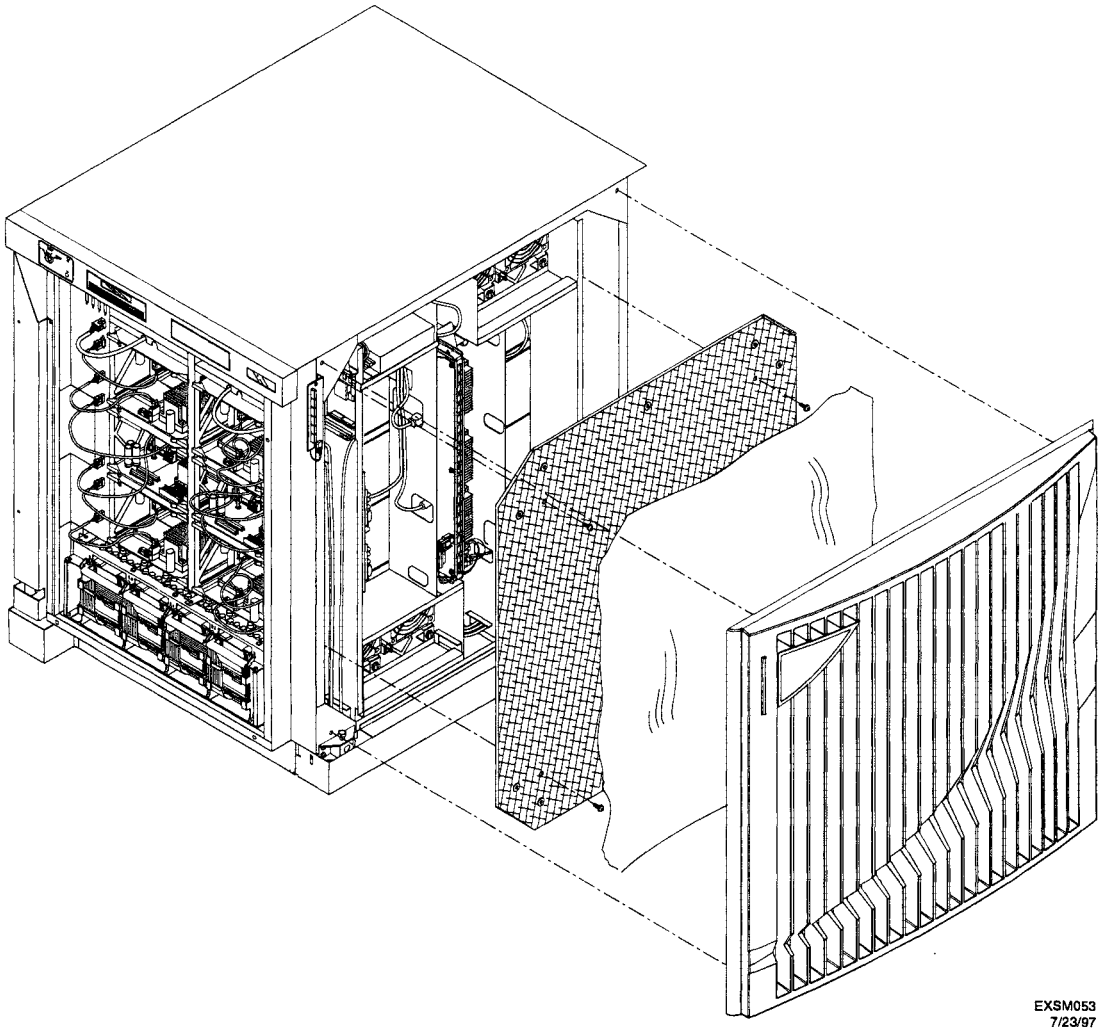


Step 4 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out. Refer to Figure 56 for details.

Step 5 Remove the filter from the front of the chassis. It is held in place with velcro.

Step 6 Remove the front EMI panel by unfastening the screws securing the panel.

Figure 56 Front skin, filter, and EMI panel removal



Note

All processor boards and memory boards plug into the node routing board. It is necessary to unplug all boards from each side before attempting to remove the node routing board.

Step 7 Detach all memory boards, processor boards and PCI cardcages from their sockets. These boards should be pulled approximately 2 inches away from the NRB.

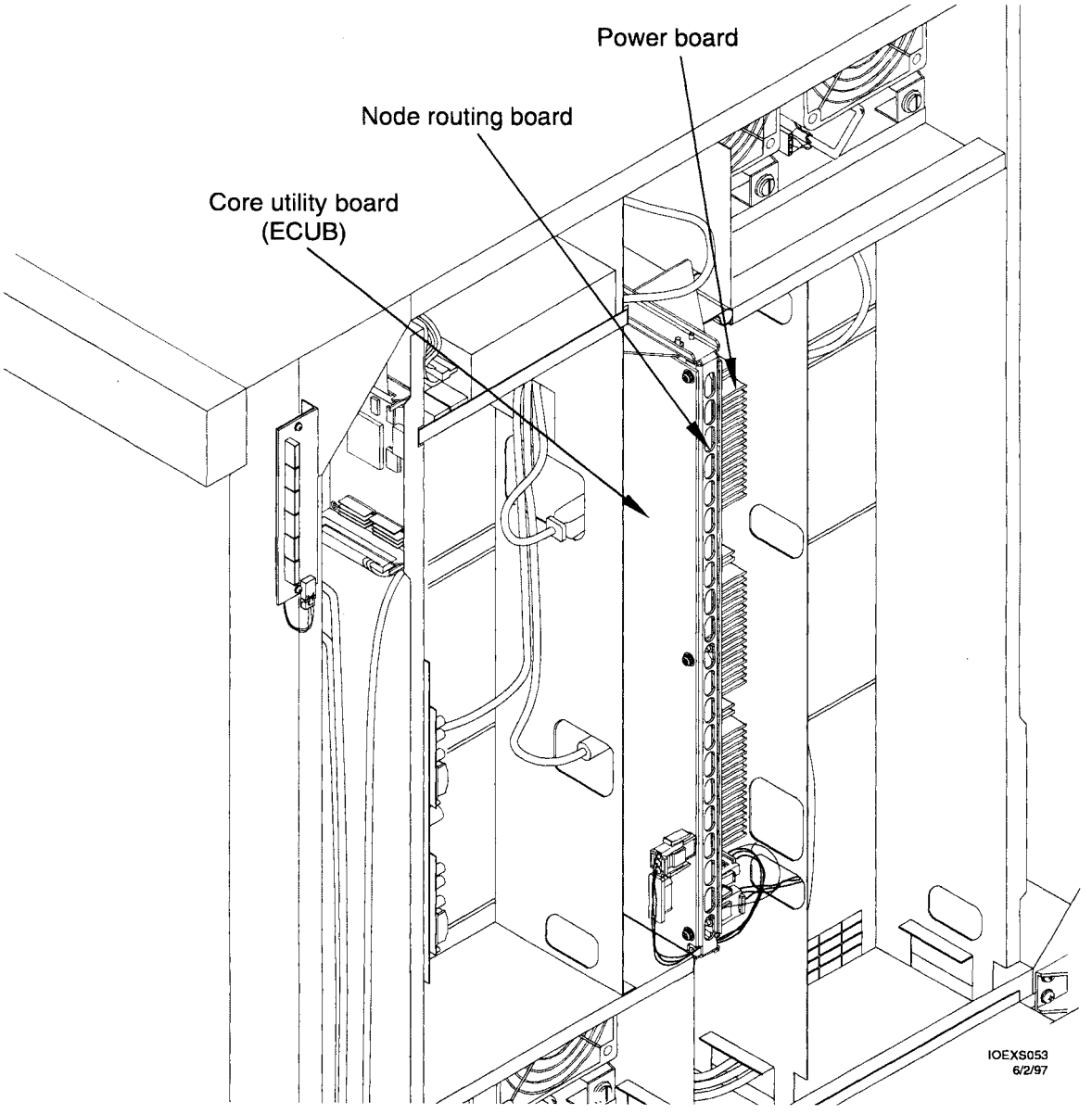
Step 8 Tag and mark the three connectors connected to the core utility board that must be removed before the node routing board can be removed. Refer to Figure 57 for core utility board location.

Step 9 Disconnect the three connectors connected to the core utility board that must be removed before the node routing board can be removed.

Step 10 Tag and mark the three connectors connected to the power board that must be removed before the node routing board can be removed. Refer to Figure 57 for power board location.

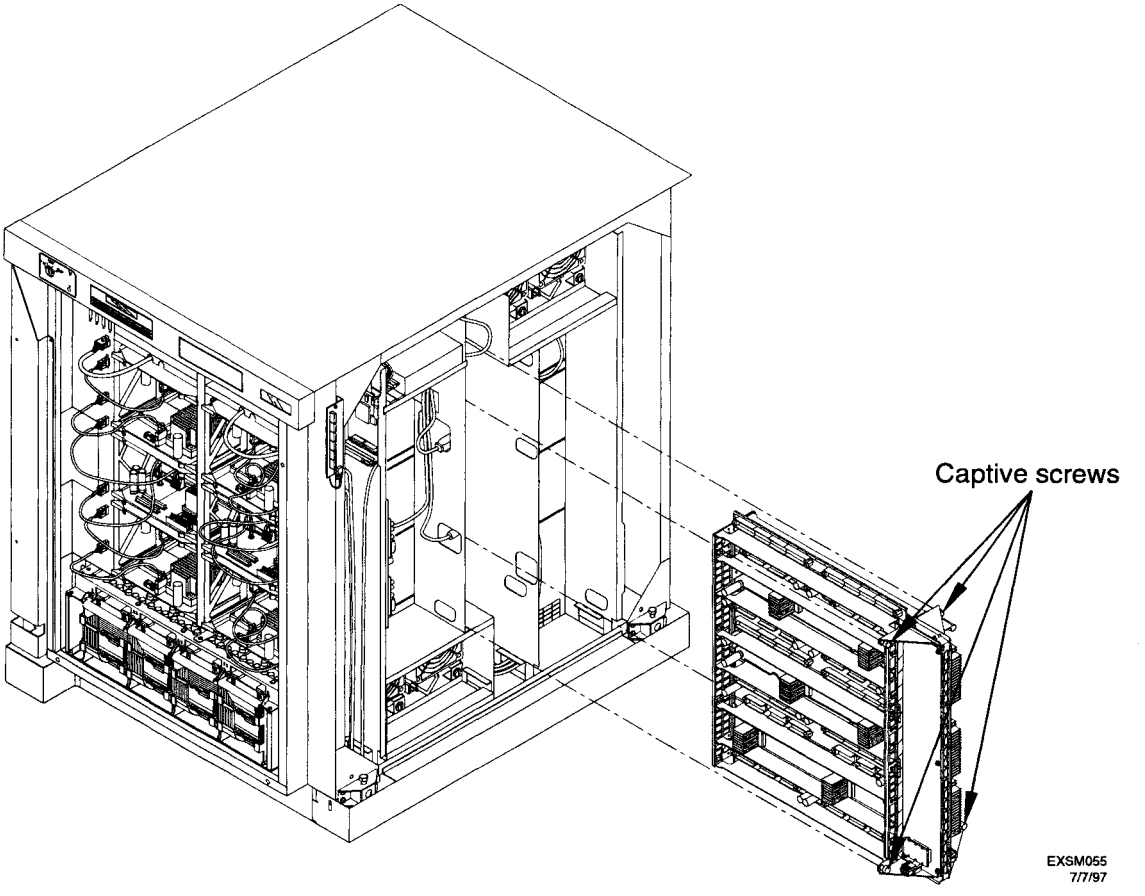
Step 11 Disconnect the three connectors connected to the power board that must be removed before the node routing board can be removed.

Figure 57 Chassis front view



Step 12 Loosen the four captive screws and carefully pull the node routing board from the chassis. Refer to Figure 58 for details.

Figure 58 Node routing board removal



Installation

This section provides the details required to install the node routing board.

Step 1 Check that all memory boards, processor boards and PCI cardcages are removed far enough to allow for ample clearance of the node routing board.

Step 2 Carefully align the node routing board in the chassis.

Step 3 Carefully slide the node routing board into the chassis ensuring that it is installed in the guide rails.

Step 4 Tighten the four captive screws. Refer to Figure 58 for details.

Step 5 Locate and connect the three connectors previously tagged and marked that connect to the core utility board. Refer to Figure 57 for core utility board location.

Step 6 Locate and connect the three connectors previously tagged and marked that connect to the power board.

Step 7 Seat all memory boards and processor boards on both the left and right side of the chassis.

Step 8 Install the side EMI panels. Use four screws on each panel.

Step 9 Install the side skins.

Step 10 Install the front EMI panel. Use four screws.

Step 11 Install the filter.

Step 12 Install the front skin.

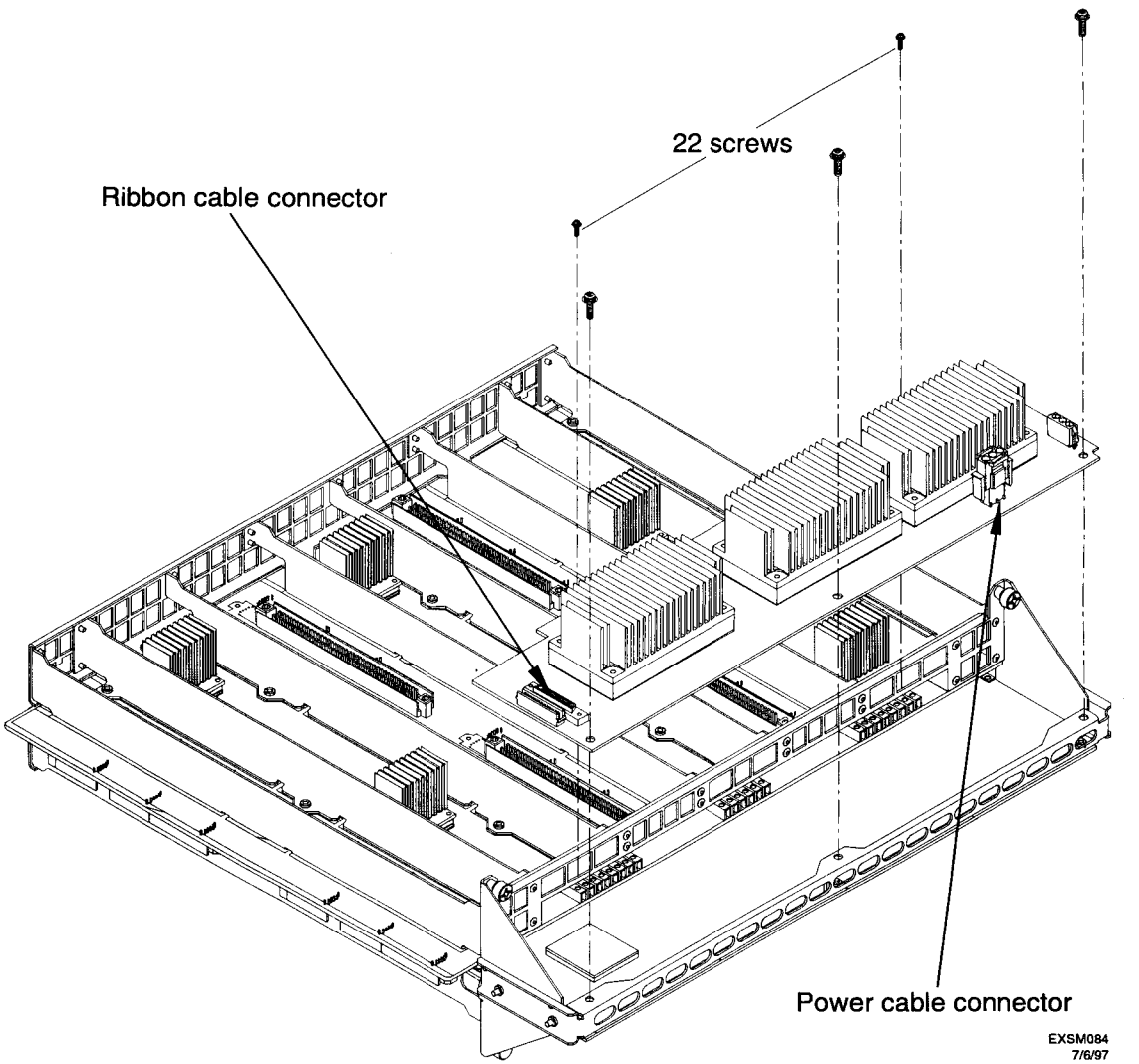
Node routing board power board

The following sections provide the information required to remove and install the node routing board power board.

Removal

This section provides the details required to remove the node routing board power board. Refer to Figure 59 for details.

Figure 59 Node routing board power board removal



Step 1 Remove the power cable from the power cable connector.

Step 2 Remove the ribbon cable from the ribbon cable connector.

Step 3 Remove three screws from the leading edge of the power board.

Step 4 Remove 22 screws from the back edge of the power board.

Step 5 Carefully lift the power board straight up to disengage it from the node routing board.

Step 6 Remove the power board from the node routing board.

Installation

This section provides the details required to install the node routing board power board. Refer to Figure 59 for details.

Step 1 Position the power board in place on the node routing board.

Step 2 Loosely install the 22 screws in the back edge of the power board.

Step 3 Install the three screws on the leading edge of the power board.

Step 4 Tighten the 22 screws on the back edge of the power board.

Step 5 Connect the ribbon cable and the power cable.

Step 6 Connect the power cable.

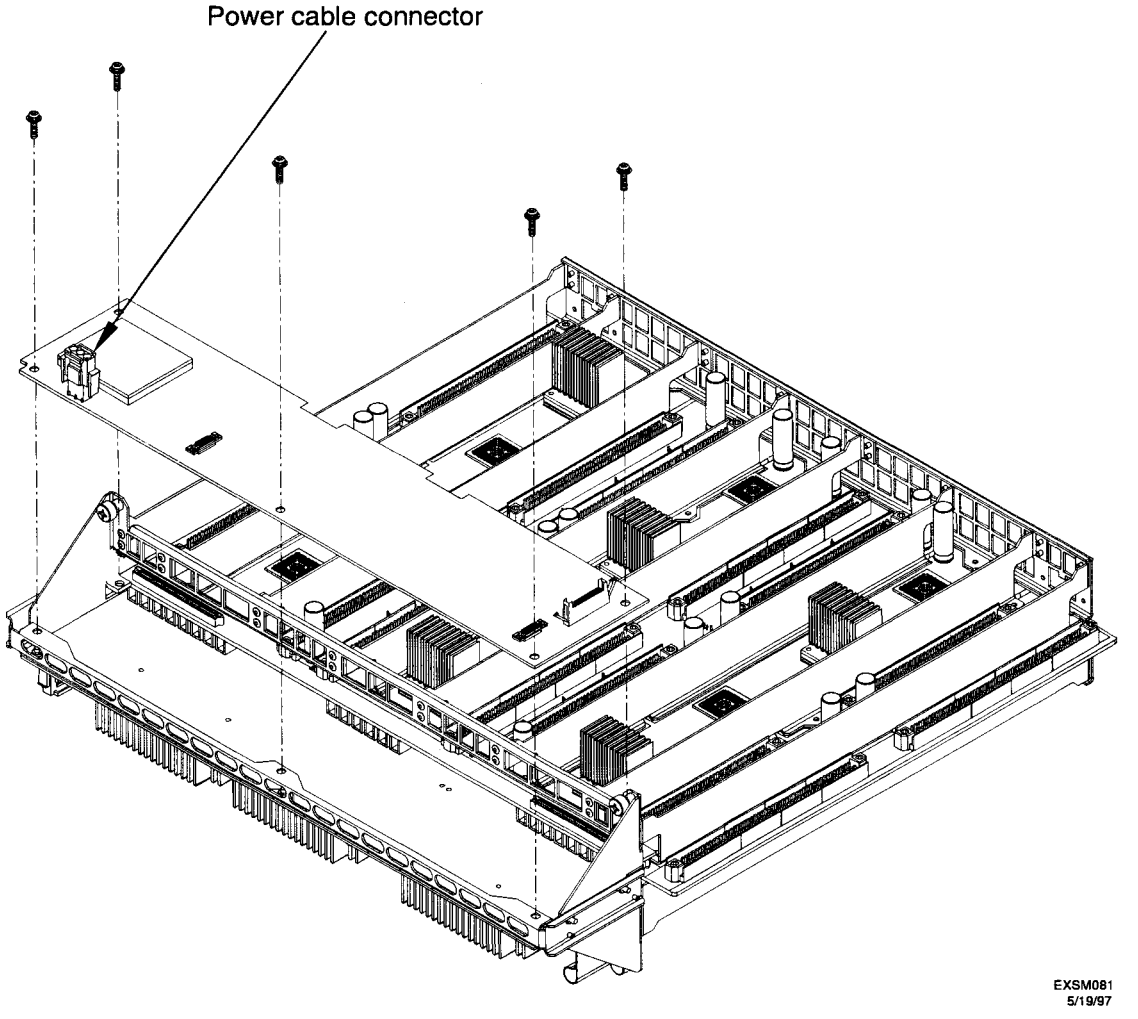
Node routing board core utility board (ECUB)

The following sections provide the information required to remove and install the node routing board core utility board.

Removal

This section provides the details required to remove the node routing board core utility board. Refer to Figure 60 for details.

Figure 60 Node routing board core utility board removal



Step 1 Remove the power cable from the power cable connector.

Step 2 Remove three screws from the leading edge of the core utility board.

Step 3 Remove two screws from the back edge of the core utility board.

Step 4 Carefully lift the core utility board straight up to disengage it from the connectors on the node routing board.

Step 5 Remove the ribbon cable connected to the top of the board.

Step 6 Remove the power board from the node routing board.

Installation

This section provides the details required to install the node routing board core utility board. Refer to Figure 60 for details.

Step 1 Position the power board in place on the node routing board.

Step 2 Connect the ribbon cable to the top of the board.

Step 3 Cause the connectors on the bottom of the core utility board to mate with the connectors on the node routing board.

Step 4 Install the three screws on the leading edge of the core utility board.

Step 5 Install the two screws on the back edge of the core utility board.

Step 6 Connect the power cable.

Embedded disk

The following sections provide the information required to remove and install the embedded disk.

Removal

This section provides the details required to remove the embedded disk.

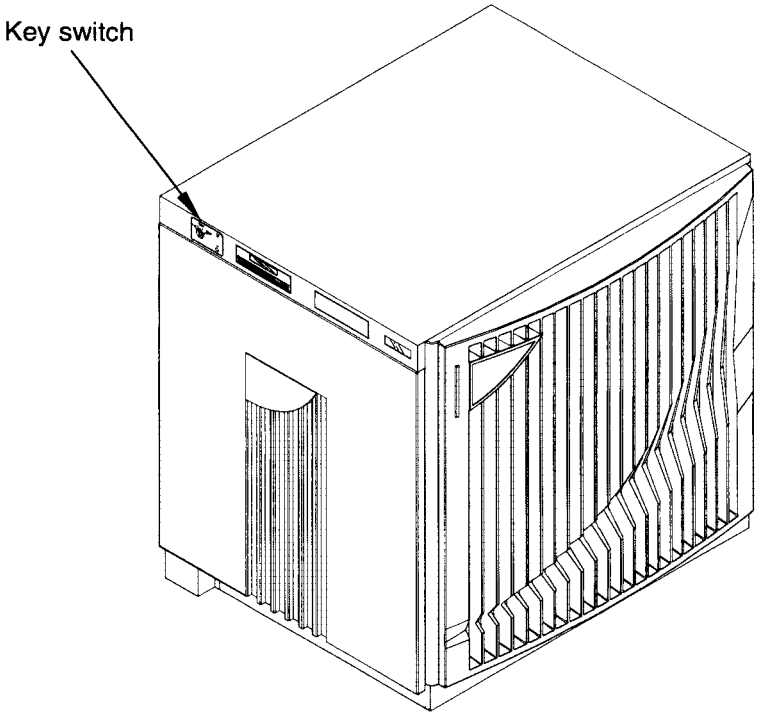
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 61 for keyswitch location.

Figure 61 Keyswitch location



Note

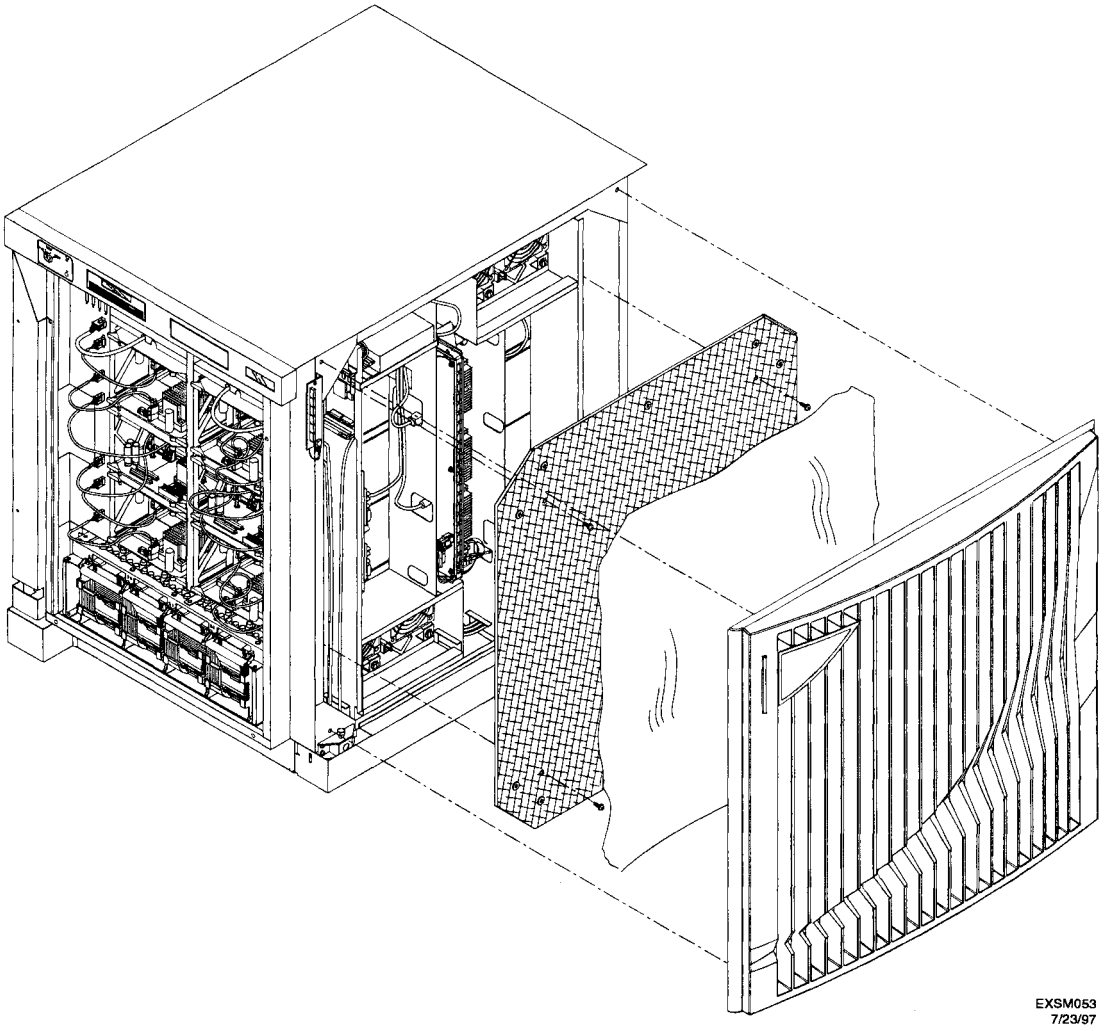
Turn off power to the system before you remove the embedded disk. Failure to remove power before removing the embedded disk will damage electronic components.

Step 3 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out. Refer to Figure 62 for details.

Step 4 Remove the filter from the front of the chassis. It is held in place with velcro.

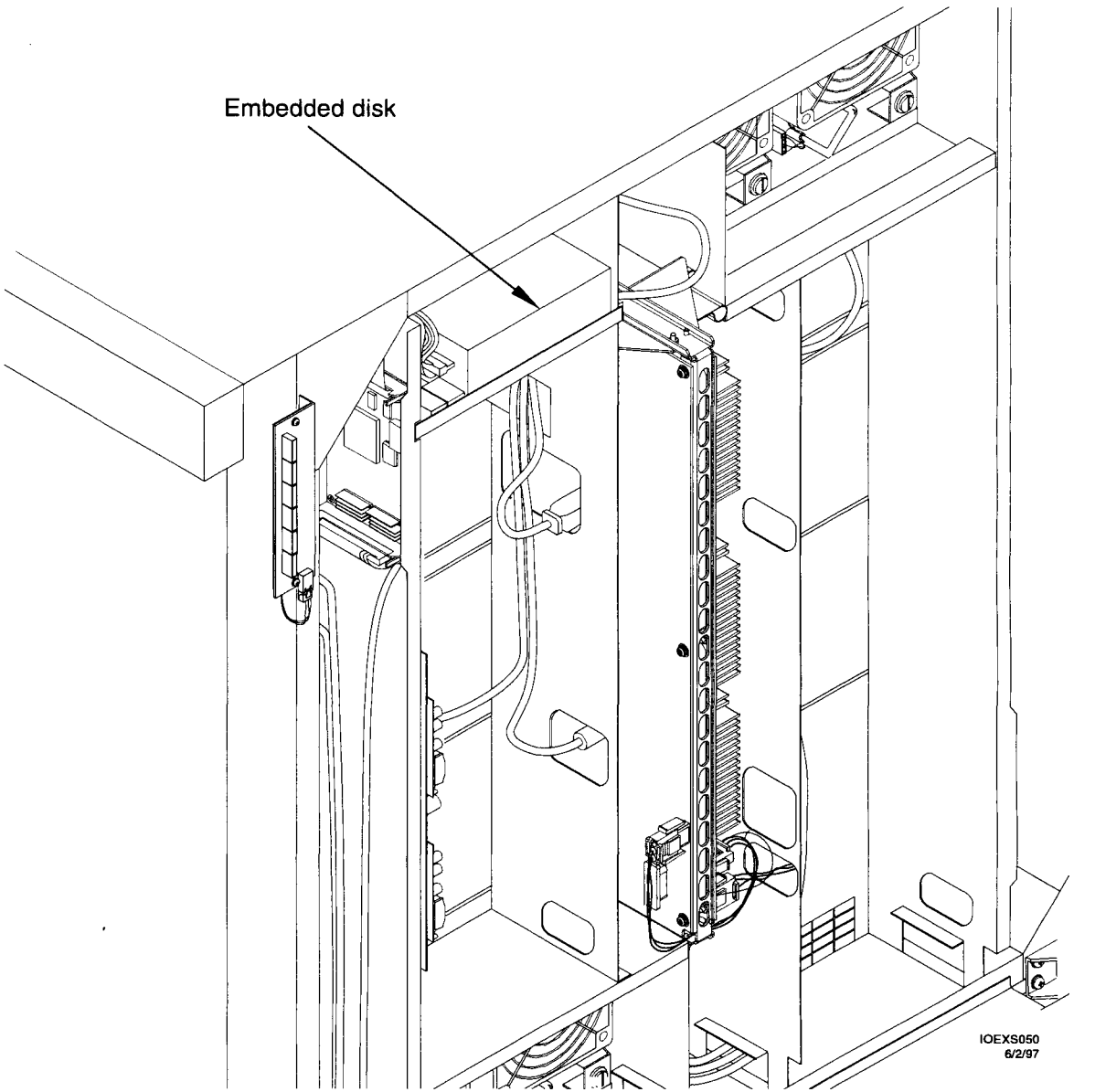
Step 5 Remove the front EMI panel by unfastening the screws securing the panel.

Figure 62 Front skin, filter, and EMI panel removal



Step 6 Locate the embedded disk in the upper left portion of the chassis. Refer to Figure 63 for details.

Figure 63 Embedded disk location

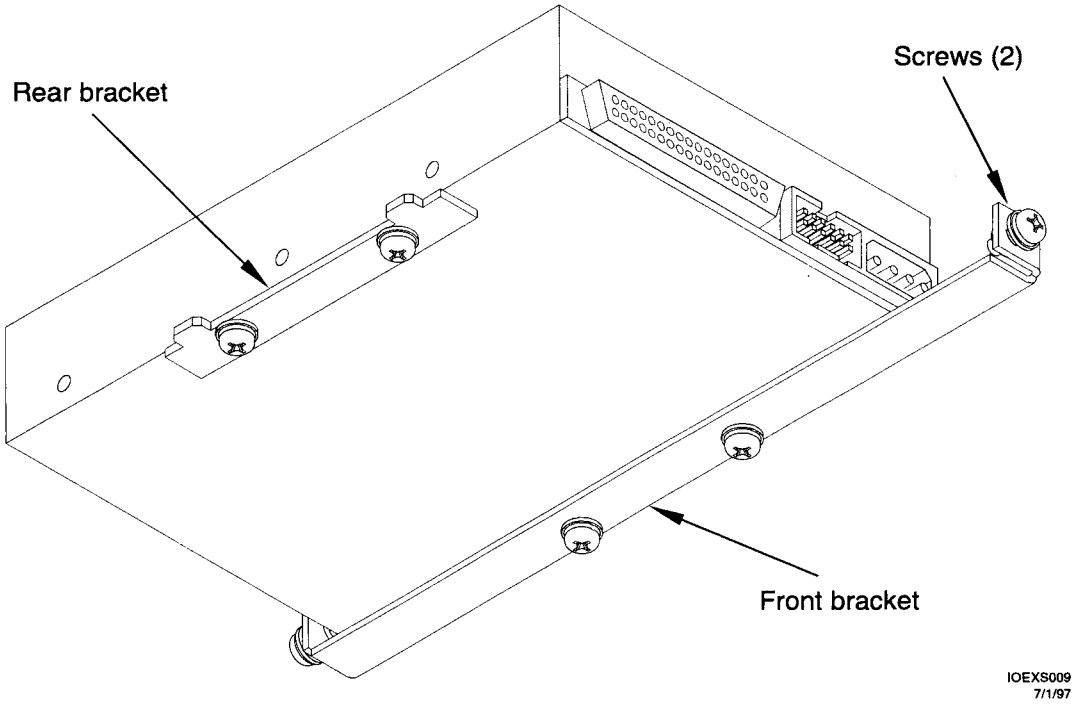


Step 7 Disconnect the SCSI cable from the disk.

Step 8 Disconnect the dc power cable from the disk.

Step 9 Remove the two front bracket screws. Refer to Figure 64 for details.

Figure 64 Embedded disk and bracket



Step 10 Lift up the embedded disk drive from under the front bracket and slide it out of the chassis.

Installation

This section provides the details required to install the embedded disk.

Note

The replacement disk drive comes complete with brackets installed.

Step 1 Ensure that the SCSI jumper settings are the same as those of the removed disk drive.

Step 2 Position the disk in the chassis. Ensure that the two tabs of the embedded disk drive rear bracket mate with the two holes of the chassis wall.

Step 3 Ensure that the front bracket slides into the frame slots provided. Secure with two screws.

Step 4 Connect the SCSCI cable to the front of the disk drive.

Step 5 Connect the dc power cable to the front of the disk drive.

Step 6 Install the front EMI panel. Use four screws.

Step 7 Install the filter.

Step 8 Install the front skin.

Embedded disk power module

The following sections provide the information required to remove and install the embedded disk power module.

Removal

This section provides the details required to remove the embedded disk power module.

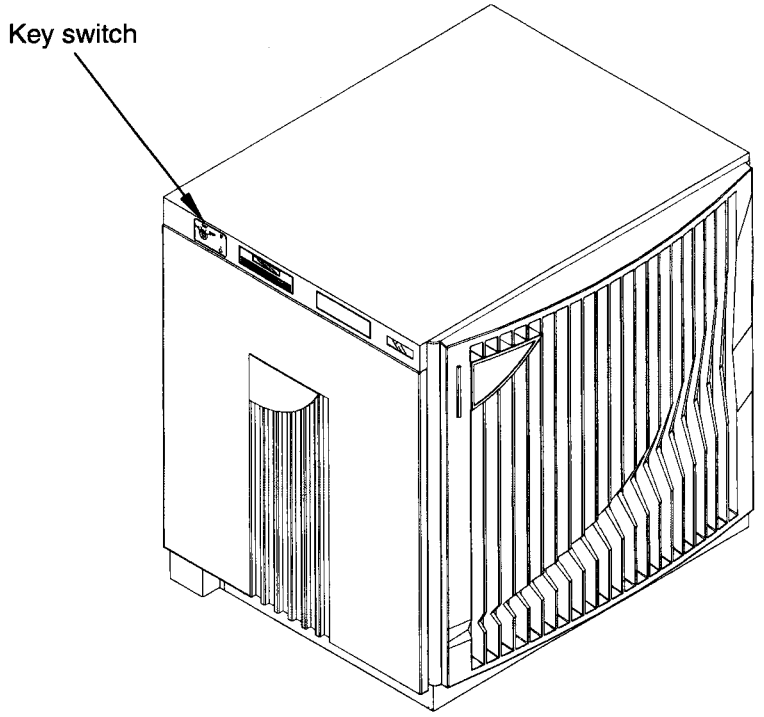
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 65 for keyswitch location.

Figure 65 Keyswitch location



Note

Turn off power to the system before you remove the power module. Failure to remove power before removing the power module will damage electronic components.

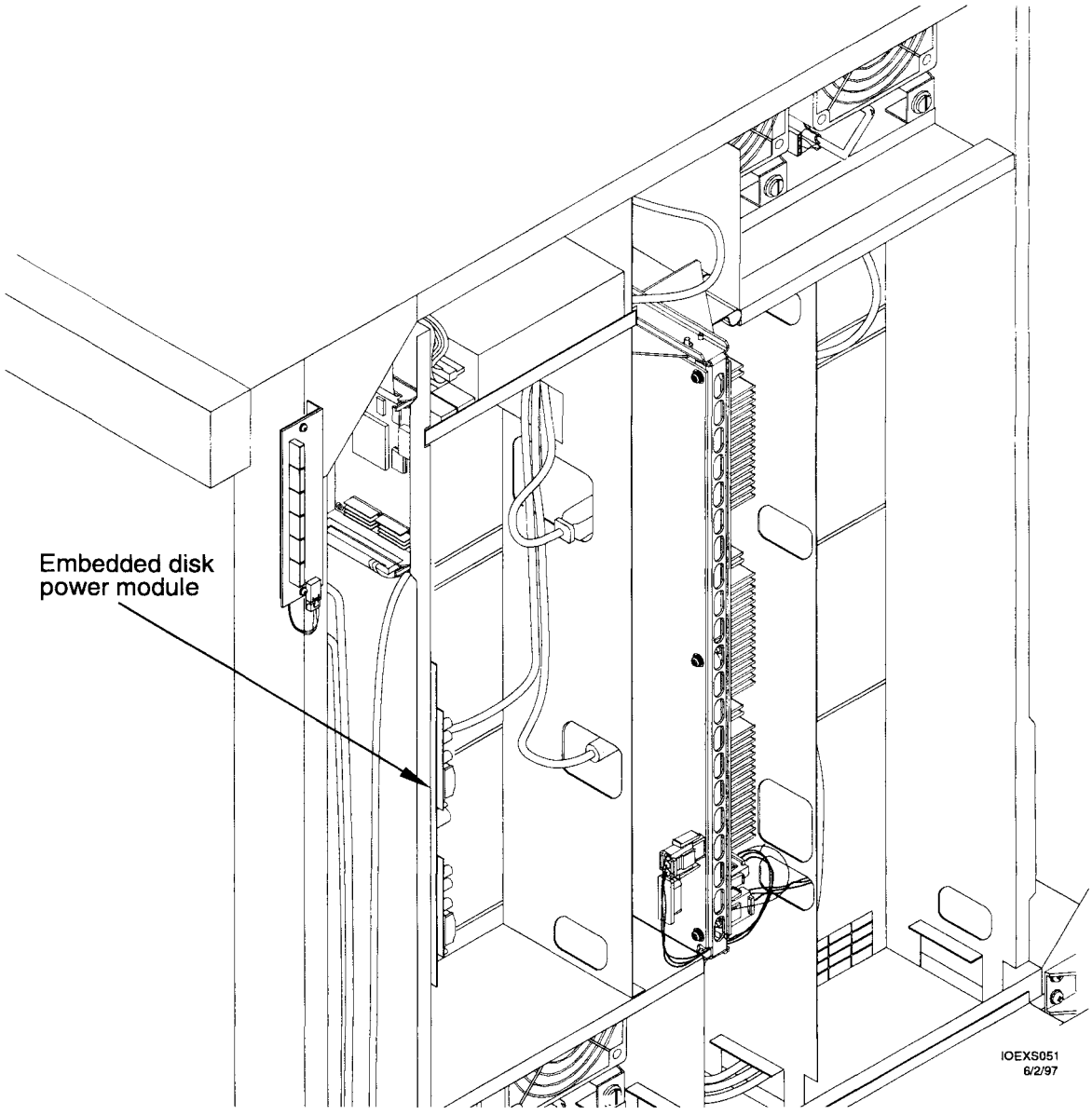
Step 3 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out. Refer to Figure 62 for details.

Step 4 Remove the filter from the front of the chassis. It is held in place with velcro.

Step 5 Remove the front EMI panel by unfastening the screws securing the panel.

Step 6 Locate the embedded disk drive power module in the upper left portion of the chassis. Refer to Figure 66 for location details.

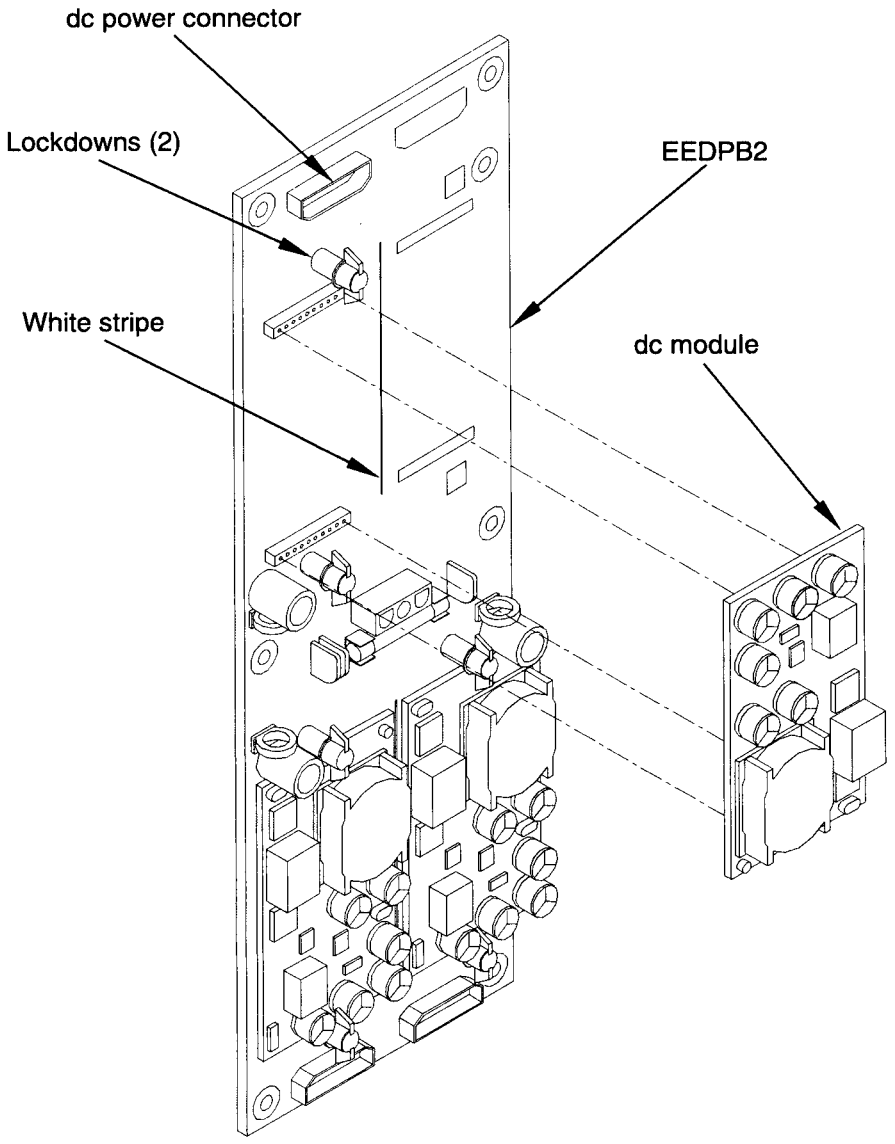
Figure 66 Embedded disk power module location



Step 7 Turn the two lockdowns until they are no longer restricting the power card movement. Refer to Figure 67 for power card removal details.

Step 8 Remove the power module.

Figure 67 Embedded disk power module removal



Installation

This section provides the details required to install the embedded disk. Refer to Figure 67 for details.

Step 1 Position the power module on the power board. Ensure that the left edge of the power module is lined up with the outer edge of the power board and that the right edge is lined up with the white stripe.

Step 2 Turn the lockdowns to a position that secures the power module to the power board.

Step 3 Install the front EMI panel. Use four screws.

Step 4 Install the filter.

Step 5 Install the front skin.

Powersupply (NPS)

The following sections provide the information required to remove and install the power supply. There are two methods by which the power supplies can be replaced.

Preferred replacement method

Removal

This section provides the details required to remove the power supply.

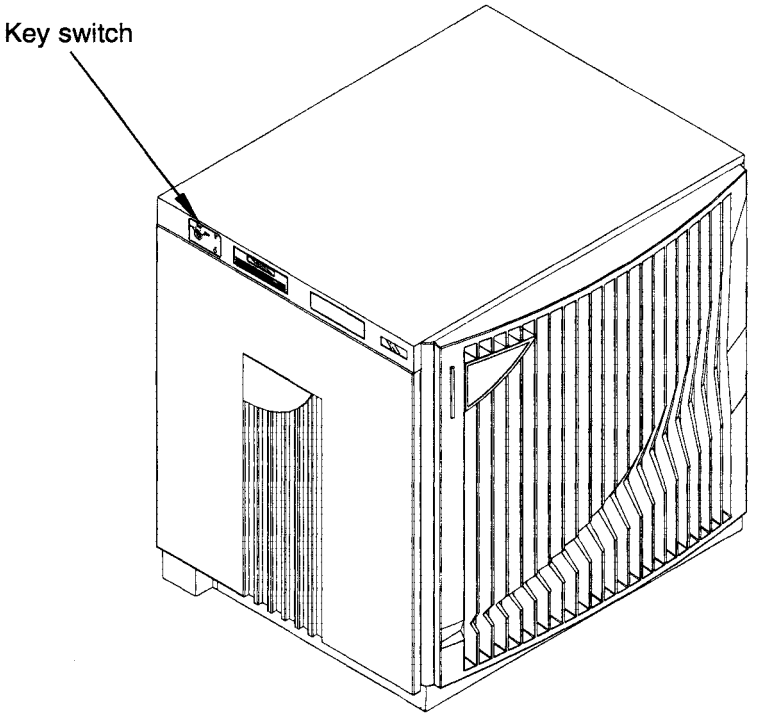
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 68 for keyswitch location.

Figure 68 Keyswitch location



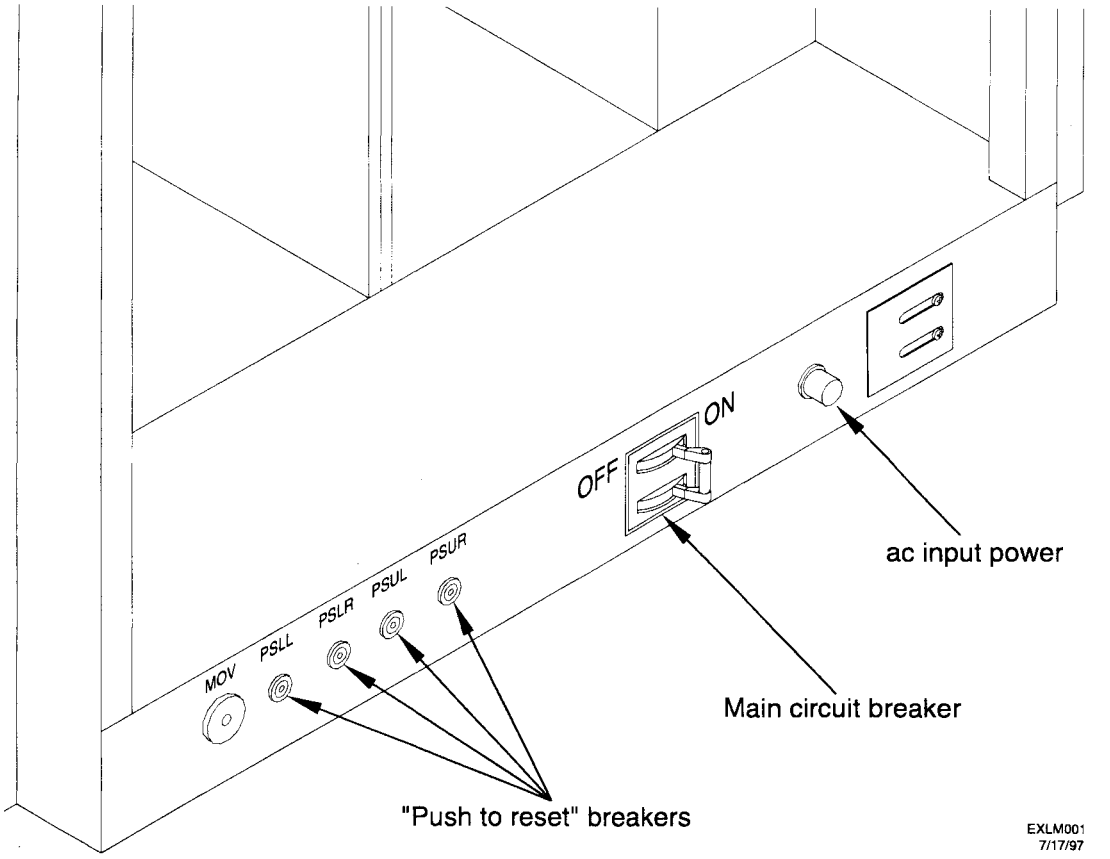
Note

Turn off power to the system before you remove the power supply. Failure to remove power before removing the power supply will damage electronic components.

Step 3 Remove the right side skin by pulling from the top and bottom of the skin until it pops out.

Step 4 Set the main circuit breaker to **OFF**. Refer to Figure 69, for circuit breaker location.

Figure 69 Main circuit breaker location

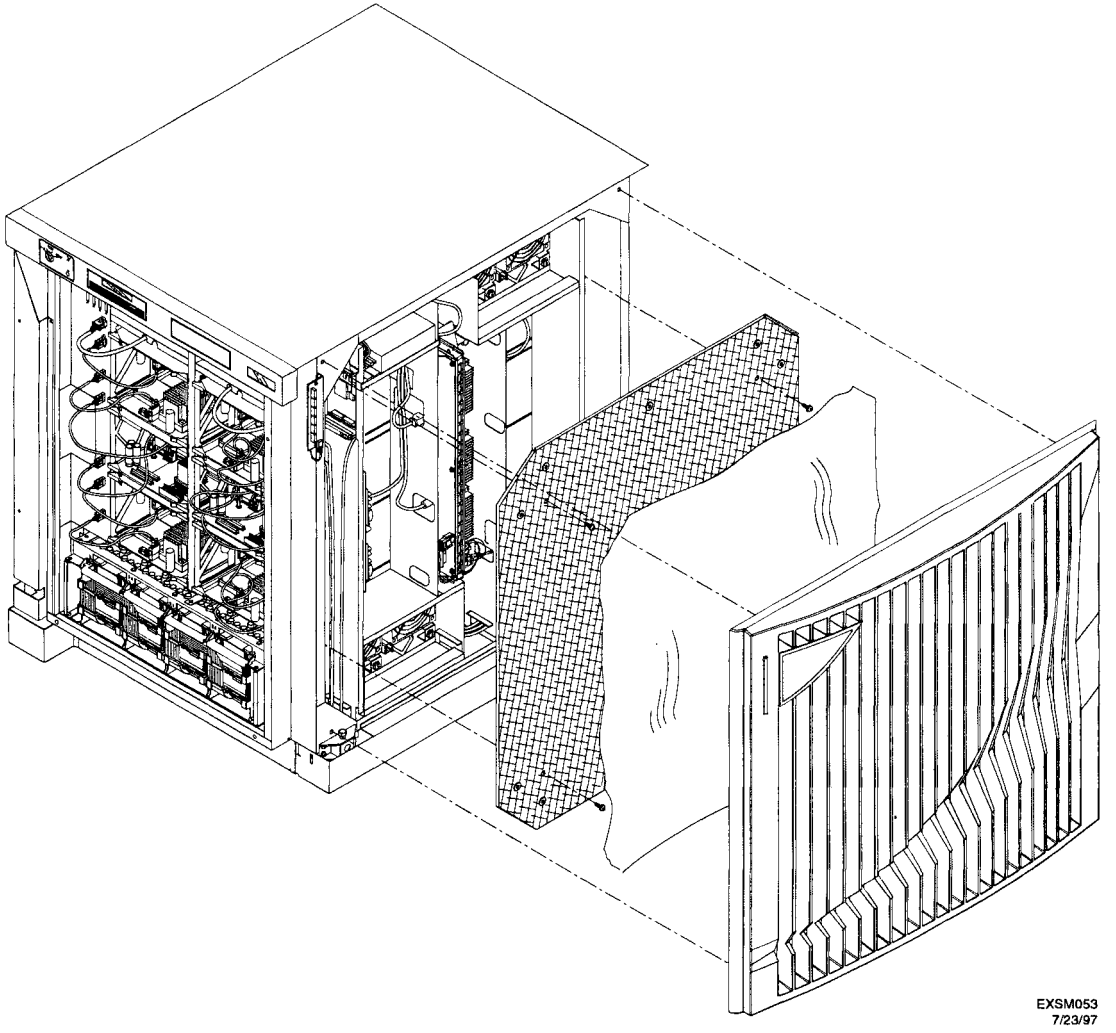


Step 5 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out. Refer to Figure 70 for details.

Step 6 Remove the filter from the front of the chassis. It is held in place with velcro.

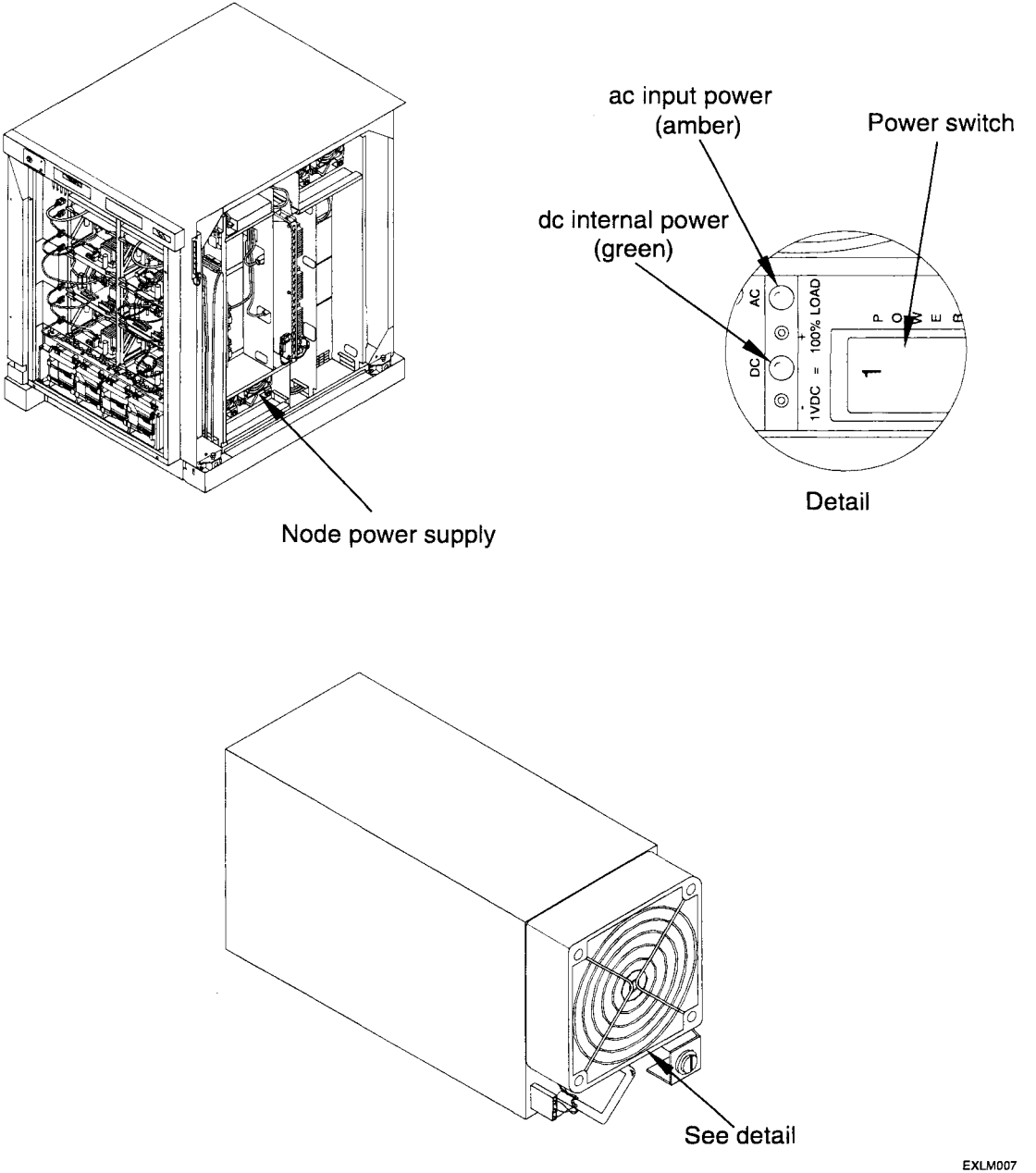
Step 7 Remove the front EMI panel by unfastening the screws securing the panel.

Figure 70 Front skin, filter, and EMI panel removal



Step 8 Locate the power supply. Refer to Figure 71 for power supply locations.

Figure 71 Node power supply locations



Step 9 Rotate the retainer in a clockwise direction until the retaining tab rotates free from the chassis.

Step 10 Remove the power supply by pulling it straight out.

Installation

This section provides the details required to install the power supply.

Step 1 Position the power supply in the chassis.

Step 2 Slide the power supply into position taking care to seat the power connector.

Step 3 Rotate the retainer in a counterclockwise direction until the retaining tab engages the slot in the chassis.

Step 4 Set the main circuit breaker to **ON**.

Step 5 Check that the ac light on the power supply is lit.

Step 6 Install the right side skin.

Step 7 Install the front EMI panel. Use four screws.

Step 8 Install the filter.

Step 9 Install the front skin.

Warm swap method

Removal

It may be necessary to warm swap a power supply. This may be required when shutting down the system is not desirable.

This section provides the details required to remove the power supply in a warm swap condition.

Caution

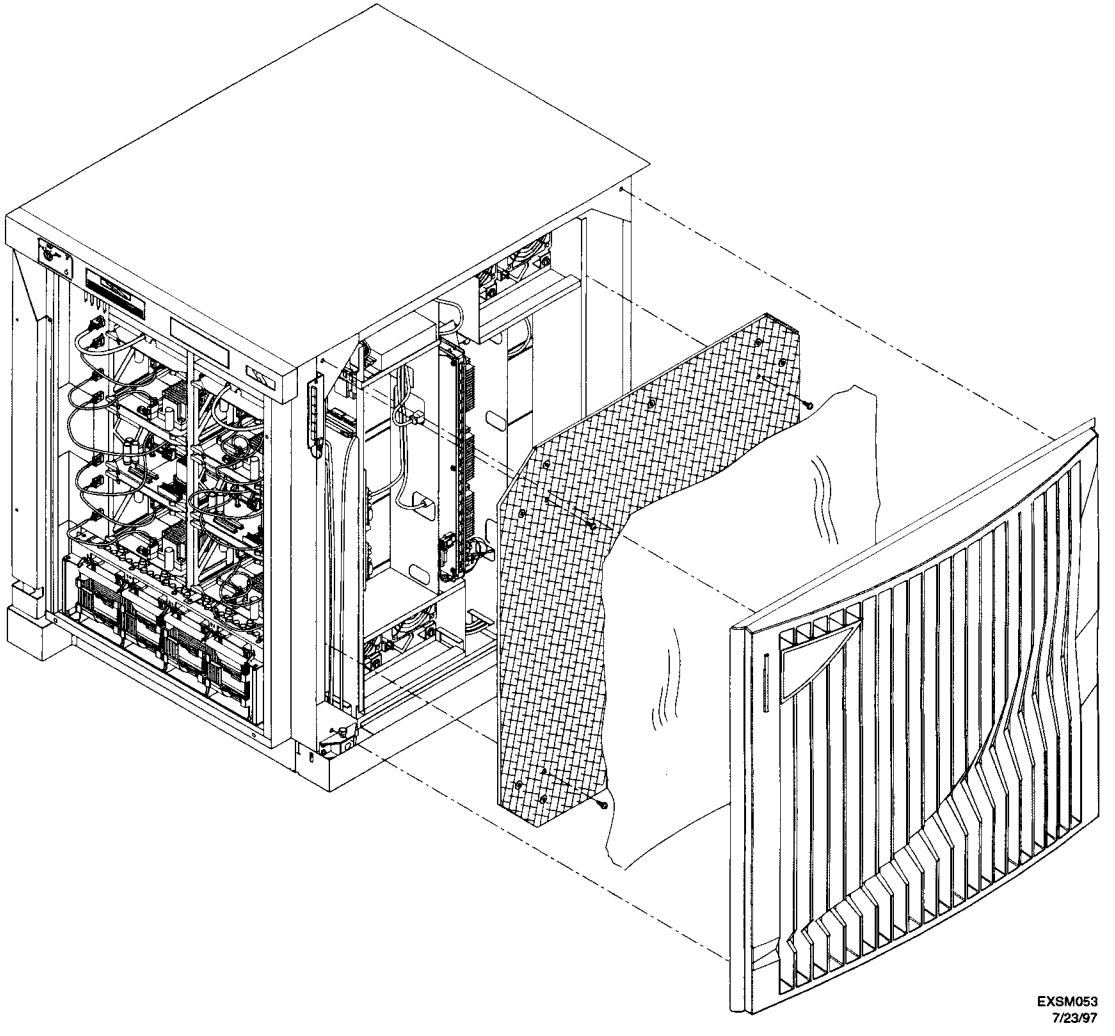
RISK OF FIRE:
48V power supplies (Node Power Supplies - NPS) must be switched to the off "0" position before removing or inserting into the system. Failure to do so will result in connector degradation and eventual over heating.

Step 1 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out. Refer to Figure 70 for details.

Step 2 Remove the filter from the front of the chassis. It is held in place with velcro.

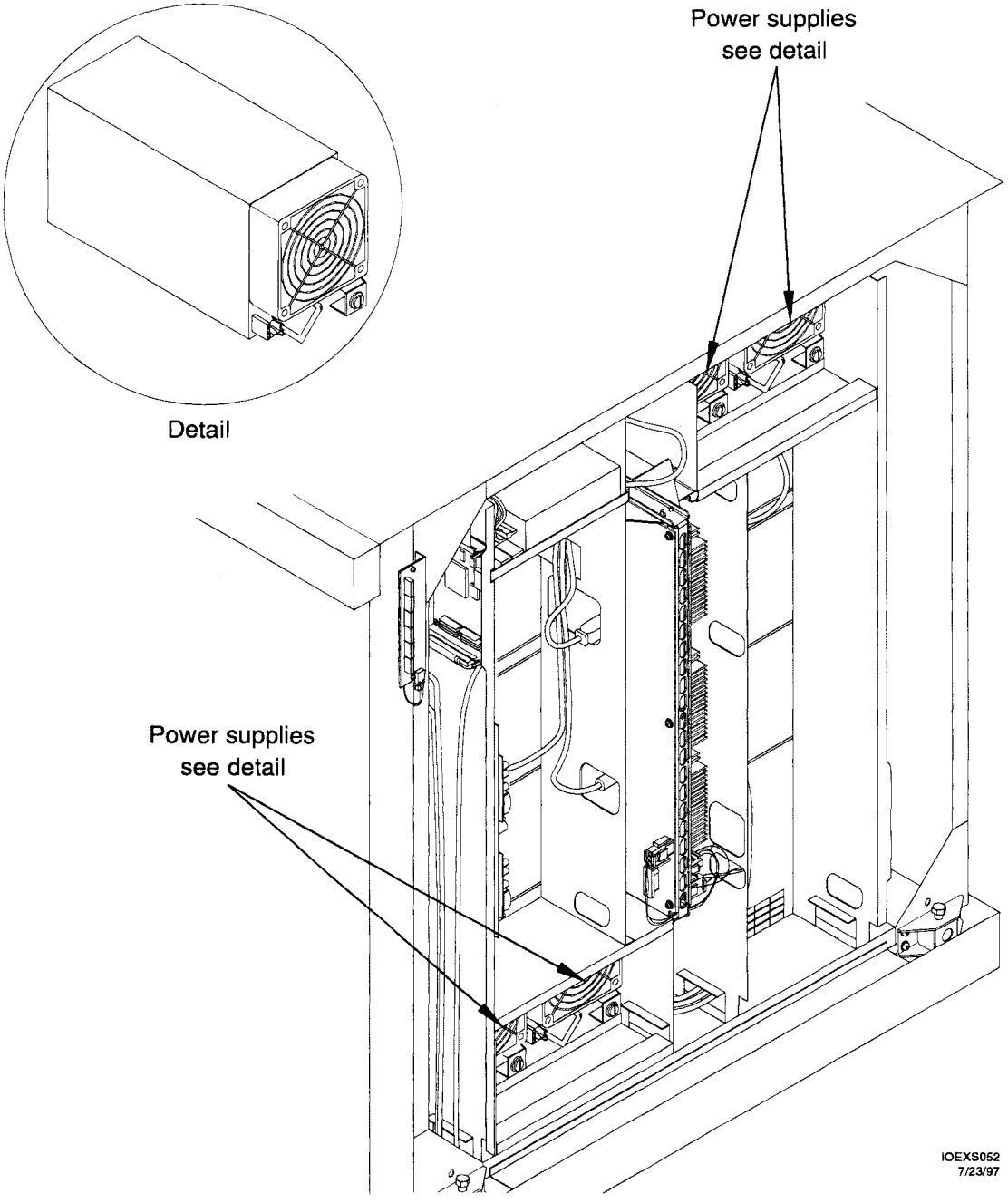
Step 3 Remove the front EMI panel by unfastening the screws securing the panel.

Figure 72 Front skin, filter, and EMI panel removal



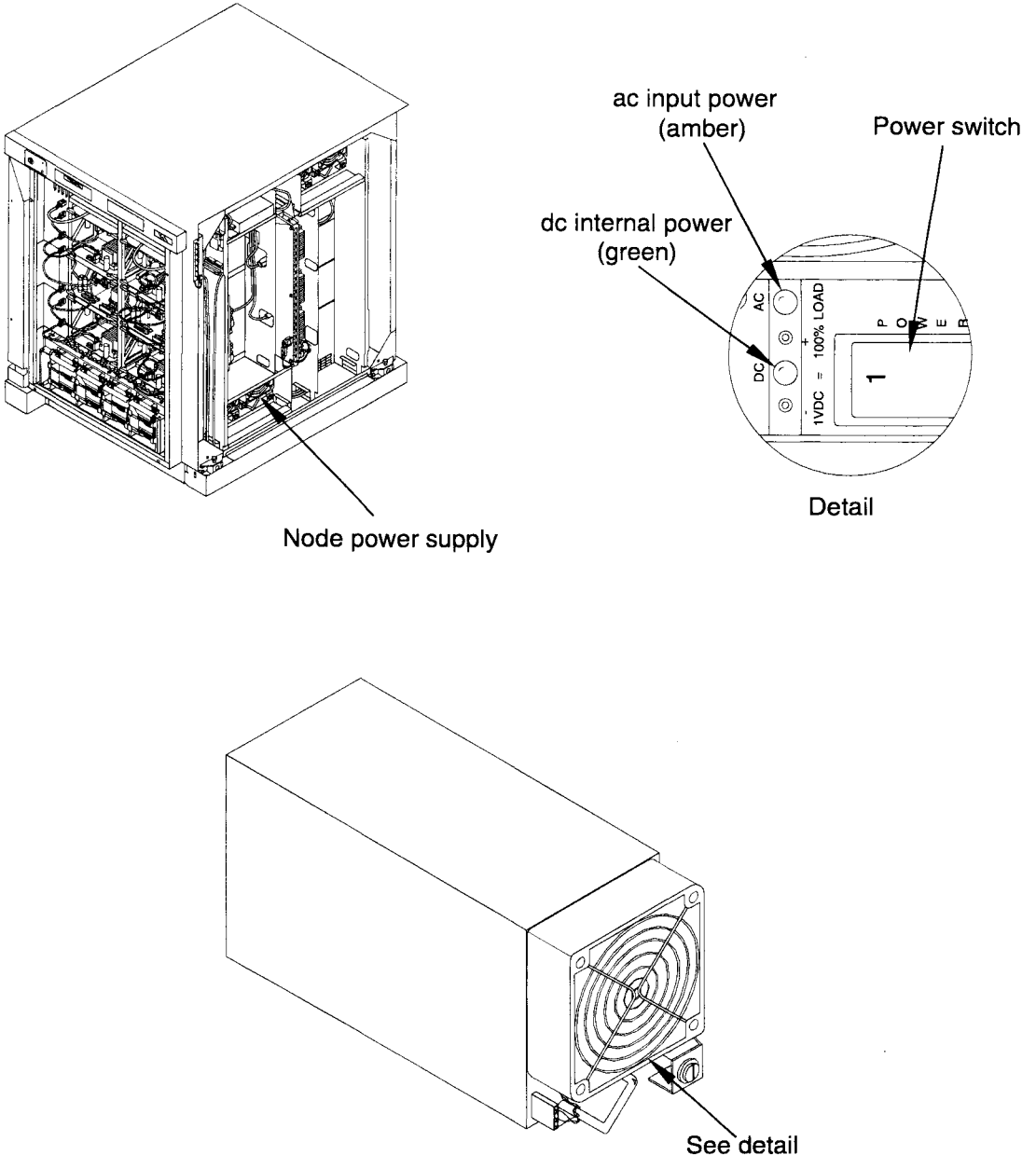
Step 4 Locate the power supply. Refer to Figure 71 for power supply locations.

Figure 73 Node power supply locations



Step 5 Set the power supply switch to off "0". Refer to Figure 74, for details.

Figure 74 Power supply power switch location



Step 6 Rotate the retainer in a clockwise direction until the retaining tab rotates free from the chassis.

Step 7 Remove the power supply by pulling it straight out.

Installation

This section provides the details required to install the power supply in a warm swap condition.

Caution

RISK OF FIRE:
48V power supplies (Node Power Supplies - NPS) must be switched to the off "0" position before removing or inserting into the system. Failure to do so will result in connector degradation and eventual over heating.

FEUERGEFAHR
Der Ein-/Aus-Schalter der 48V Netzteile (Node Power Supply - NPS) muss in die Aus-Position "0" geschaltet werden, bevor die Netzteile aus dem System entfernt oder in dieses installiert werden. Eine Nichtbeachtung dieser Vorgabe kann zu Schaeden an den Verbindungskontakten und dadurch eventuell zu einer Ueberhitzung fuehren.

Risque d'incendie
Les alimentations 48V (Node Power Supplies - NPS) doivent commut sur la position off "0" avant d'retir du ouins es dans le systme. Le non respect de cette procdure entrainera la degradation des connecteurs et un risque de feu.

Step 1 Set the power supply switch to off "0". Refer to Figure 74, for details.

Step 2 Position the power supply in the chassis.

Step 3 Slide the power supply into position taking care to seat the power connector.

Step 4 Rotate the retainer in a counterclockwise direction until the retaining tab engages the slot in the chassis.

Step 5 Set the power supply switch to on "1".

Step 6 Check that the ac light on the power supply is lit.

Step 7 Install the right side skin.

Step 8 Install the front EMI panel. Use four screws.

Step 9 Install the filter.

Step 10 Install the front skin.

LED board

The following sections provide the information required to remove and install the LED board.

Removal

This section provides the details required to remove the LED board.

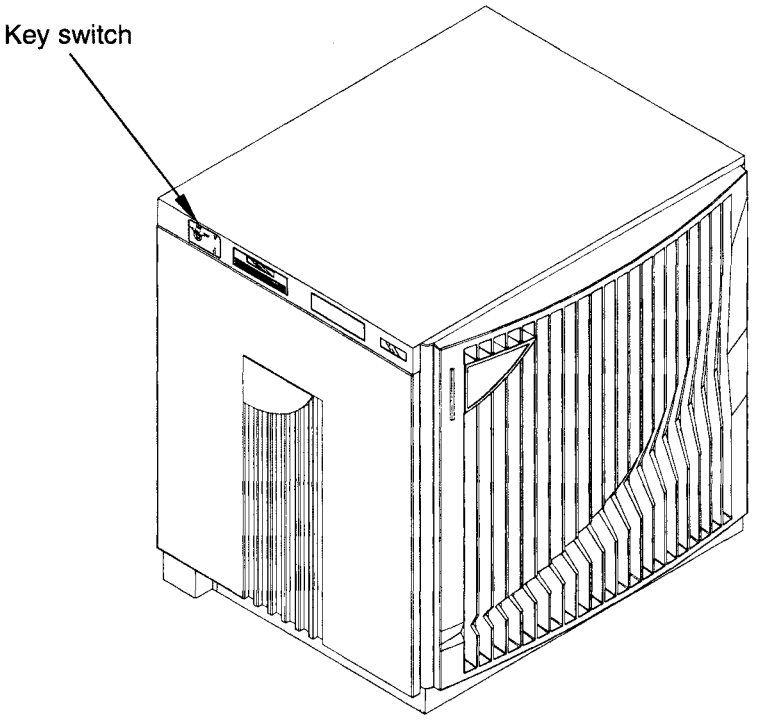
Step 1 Shut down the system with the `/etc/shutdown` command.

```
/etc/shutdown -h time
```

The time argument can be used to schedule a timed shutdown or the keyword `now` can be used to shut down the system immediately. Refer to the *SPP UX System Administrator's Guide* or the shutdown man page for more information on `/etc/shutdown`.

Step 2 Terminate power to the system by turning the keyswitch on the operator panel to the **OFF** position. Refer to Figure 75 for keyswitch location.

Figure 75 Keyswitch location



Note

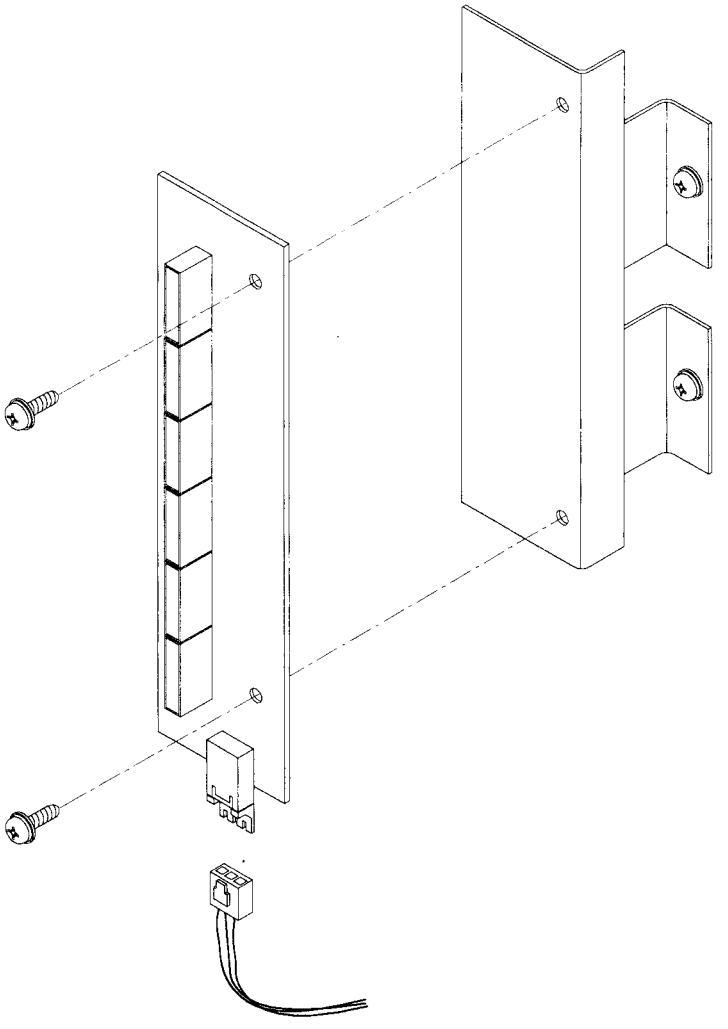
Turn off power to the system before you remove the LED board. Failure to remove power before removing the Led board will damage electronic components.

Step 3 Remove the front cabinet skin by pulling from the top and bottom of the skin until it pops out.

Step 4 Disconnect the power connector. Refer to Figure 76 for details.

Step 5 Remove the two screws securing the LED board to the bracket.

Figure 76 LED board removal



Installation

This section provides the details required to install the LED board.

Step 1 Position the LED board on the bracket and secure with two screws.

Step 2 Connect the power cable.

Step 3 Install the front cabinet skin.

Ac power filter cord assembly

The following sections provide the information required to remove and install the ac power filter cord assembly. Refer to Figure 77 for removal and installation details.

Caution

SHOCK HAZARD
Verify that the Power Cord assembly is disconnected from the supply before removing or replacing AC Power Cord assembly.

Hochspannung
Bei Arbeiten an der Versorgungsspannung besteht die Gefahr eines Stromschlages. Ausreichend isolierte Pruefspitzen benutzen. Nach Beendigung der Arbeiten unbedingt Gehaeuseklappe schliessen und verschrauben.

CHOC ELECTRIQUE
Risque dé choc électrique en vérifiant l'arrivée secteur. Utiliser des sondes correctement isolées S'assurer de remettre le couvercle de protection après avoir vérifié l'arrivée secteur.

Removal

This section provides the details required to remove the ac power cord filter assembly.

Step 1 Remove the 16 screws securing the assembly to the chassis.

Step 2 Disconnect the power connector.

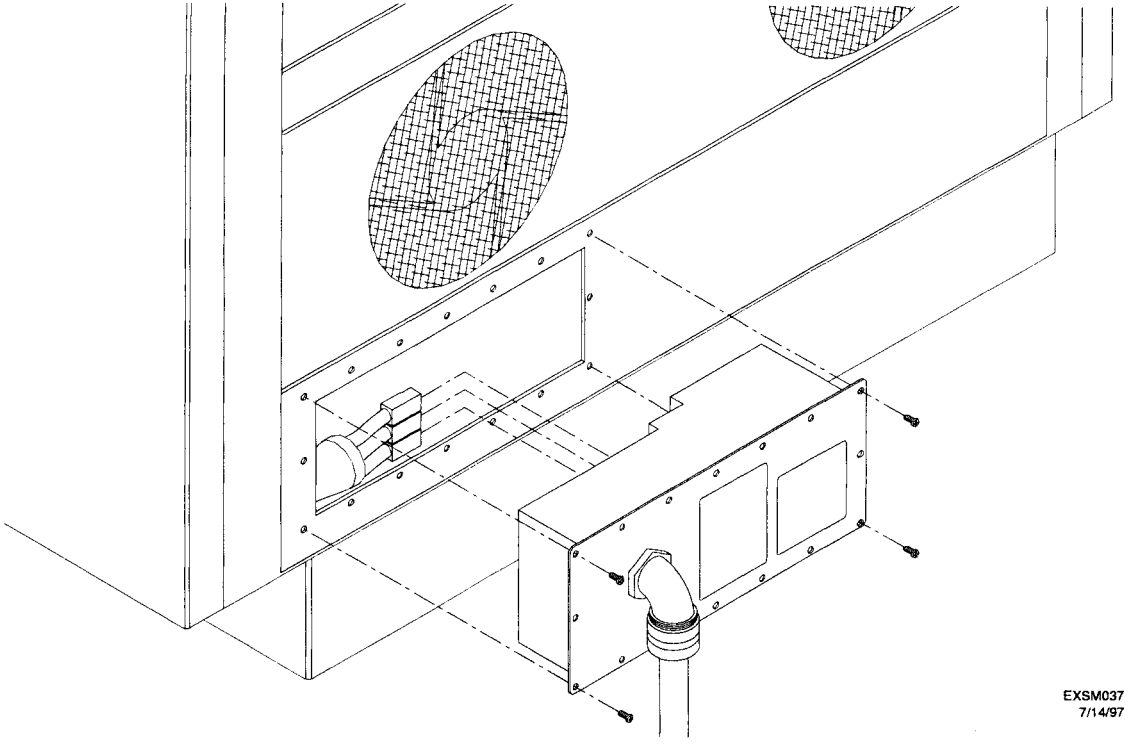
Installation

This section provides the details required to install the ac power cord filter assembly.

Step 1 Connect the power connector.

Step 2 Secure the assembly to the chassis using 16 screws.

Figure 77 Ac power cord filter assembly removal



Gate array

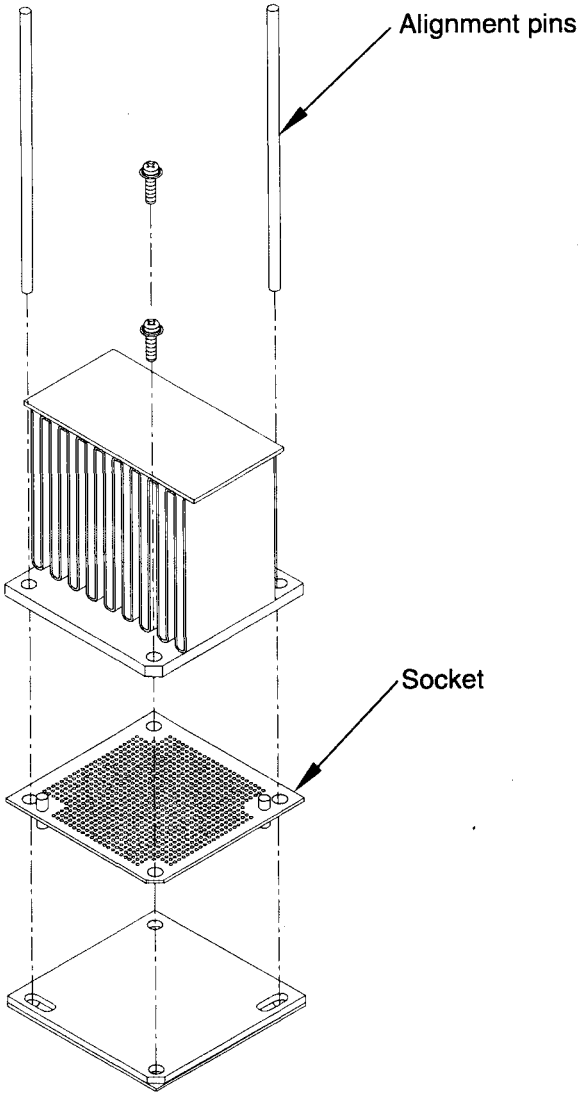
This section provides the details required to remove the gate array.

Removal

This section provides the details required to remove and install the gate array.

Step 1 Remove two screws that are opposite from each other. Use a magnetic screwdriver. Refer to Figure 78 for details.

Figure 78 Gate array removal



Step 2 Insert installation guide pins (315-000205-500) where the screws were removed.

Step 3 Remove the remaining two screws. Use a magnetic screwdriver.

Step 4 Carefully remove the gate array by sliding it up and off of the guide pins.

Step 5 Carefully remove the gate array socket by sliding it up and off of the guide pins.

Step 6 Clean the board surface using a pure bristle brush and 91% or better alcohol.

Installation

This section provides the details required to install the gate array.

Step 1 Place the new socket over the guide pins and position it on the board.

Step 2 Slide the gate array over the guide pins and position on the board.

Step 3 Install the two screw opposite each other. Install only to the point that the two screws are engaged.

Step 4 Remove the two guide pins and replace with two screws.

Step 5 Slightly tighten the screws installed in Step 3.

Step 6 Slightly tighten the screws installed in Step 4.

Step 7 Repeat the above process until all screws are snug.

Step 8 Torque all screws to 7in/lbs.

Step 9 Check the data plate on the gate array to determine the value of the delay line required. If the value is different from the gate array removed from the board, the applicable delay lines will have to be replaced.

Fuse data

A

This appendix provides all the pertinent data applicable to the fuses located within the Exemplar S-Class and X-Class servers.

General

The power portions of all node components are individually fused. It is important that that the proper fuse is used for replacement. shows the physical location of all fuses.

Fuse replacement

This section provides pertinent data for the replacement of the fuses. See Table 31 for details.

Table 31 Replacement fuse data

Location	Rating	Part number	Figure number
Core utilities board U005B4	1.5A, SB/125V	253-000147-007	Figure 79
Core utilities board U021B6·	3A, /125V	253-000147-003	Figure 79
48 volt board F1	2A, SB/250V	253-000100-004	Figure 80 Figure 81
48 volt board F2	2A, SB/250V	253-000100-004	Figure 80 Figure 81
48 volt board F3	2A, SB/250V	253-000100-004	Figure 80 Figure 81
Embedded disk power board U027F8	10A/250V	253-000128-001	Figure 82

Table 31 Replacement fuse data **(continued)**

Location	Rating	Part number	Figure number
Embedded disk power board U017J0	3A, /125V	253-000147-003	Figure 82
Embedded disk power board U023E9	3A, /125V	253-000147-003	Figure 82
Embedded disk power board U023J0	3A, /125V	253-000147-003	Figure 82
Embedded disk power board U017E9	3A, /125V	253-000147-003	Figure 82
Disk tray power board Z020D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z041D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z062D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z083D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z104D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z125D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z146D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z166D9	3A, /125V	253-000147-003	Figure 83
Disk tray power board Z166D9	20A, /500VDC	253-000152-001	Figure 83

Figure 79 Core utilities board fuse locations

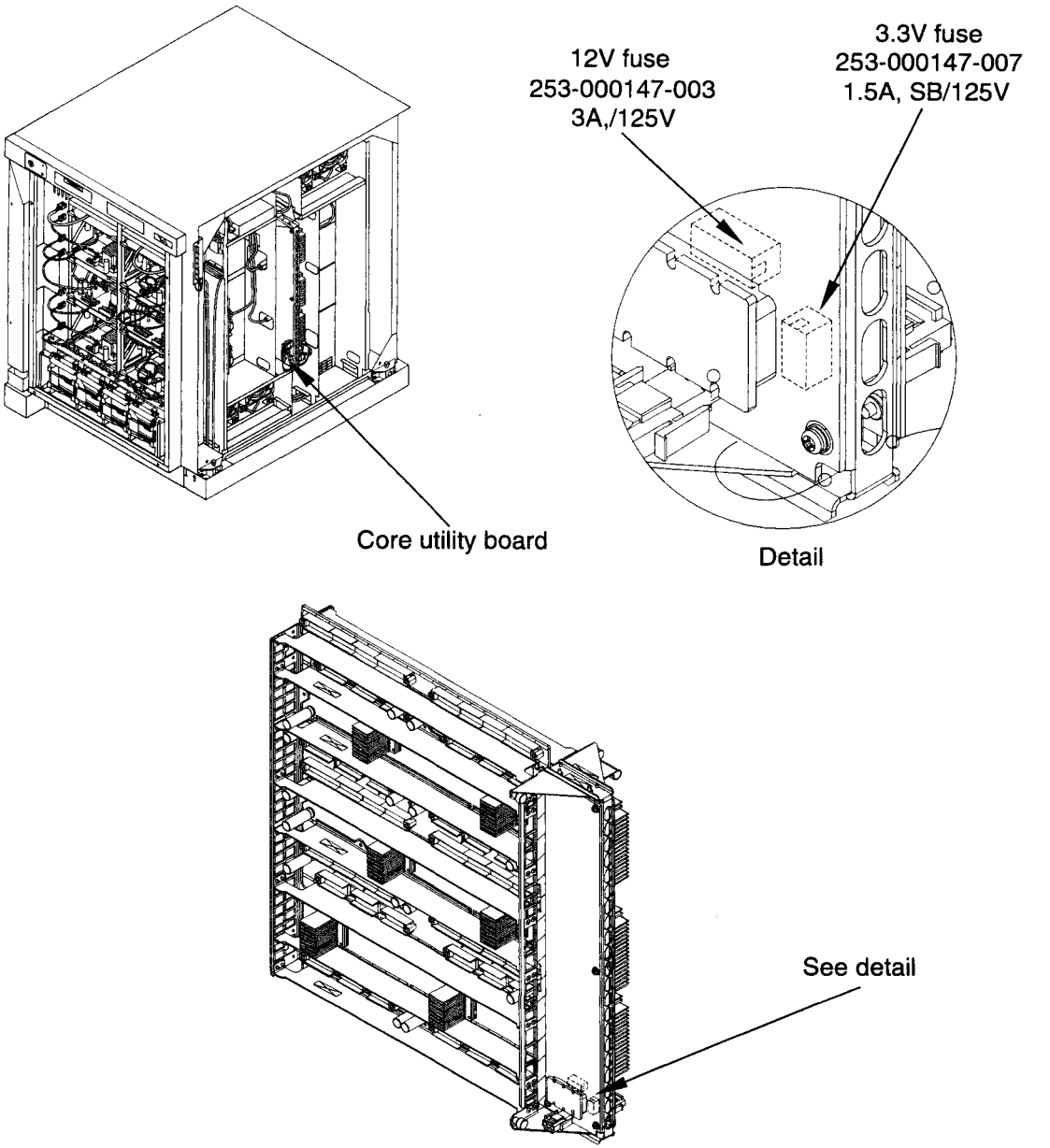


Figure 80 48 volt board fuse usage

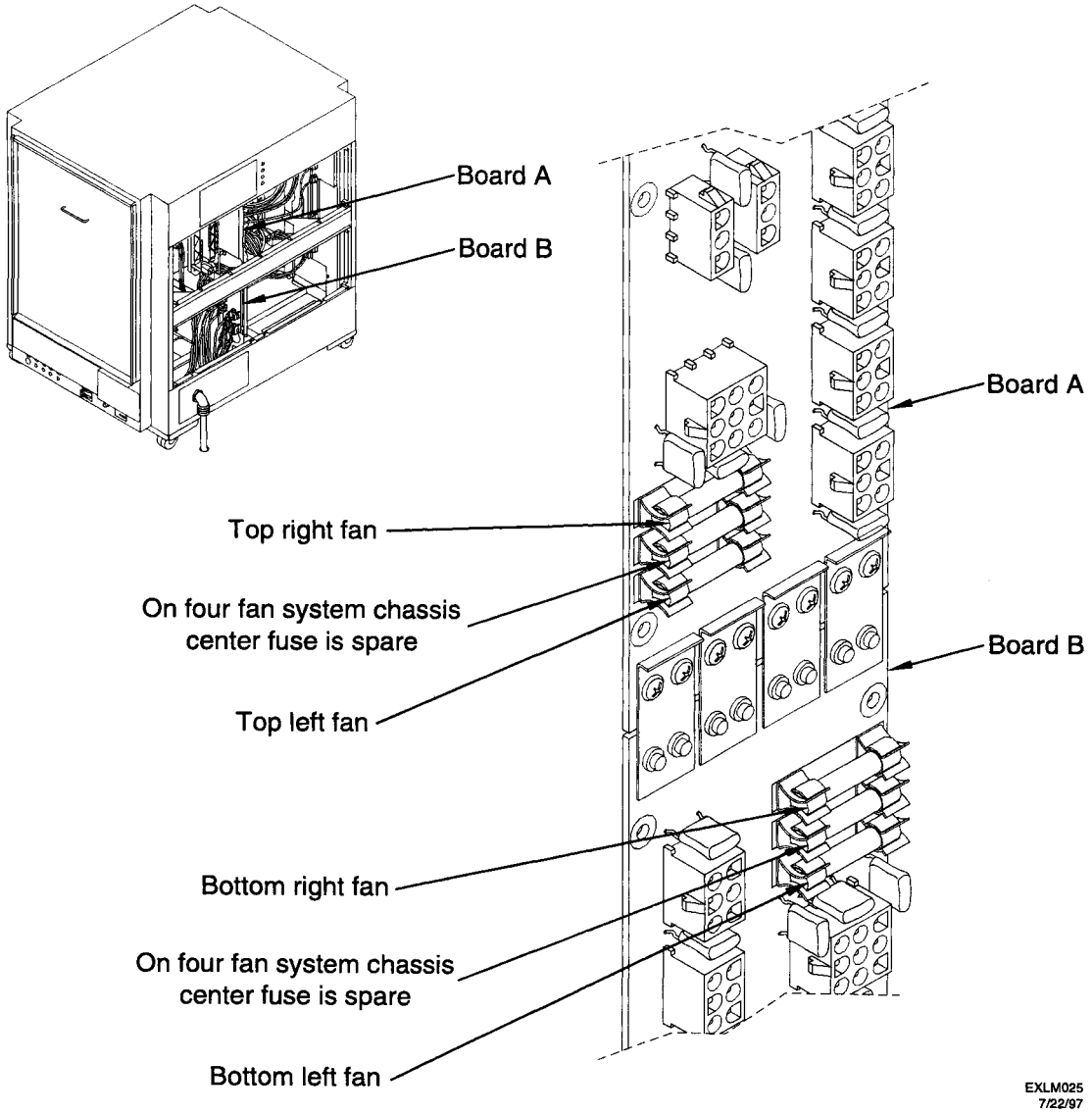


Figure 81 48 volt board fuse locations

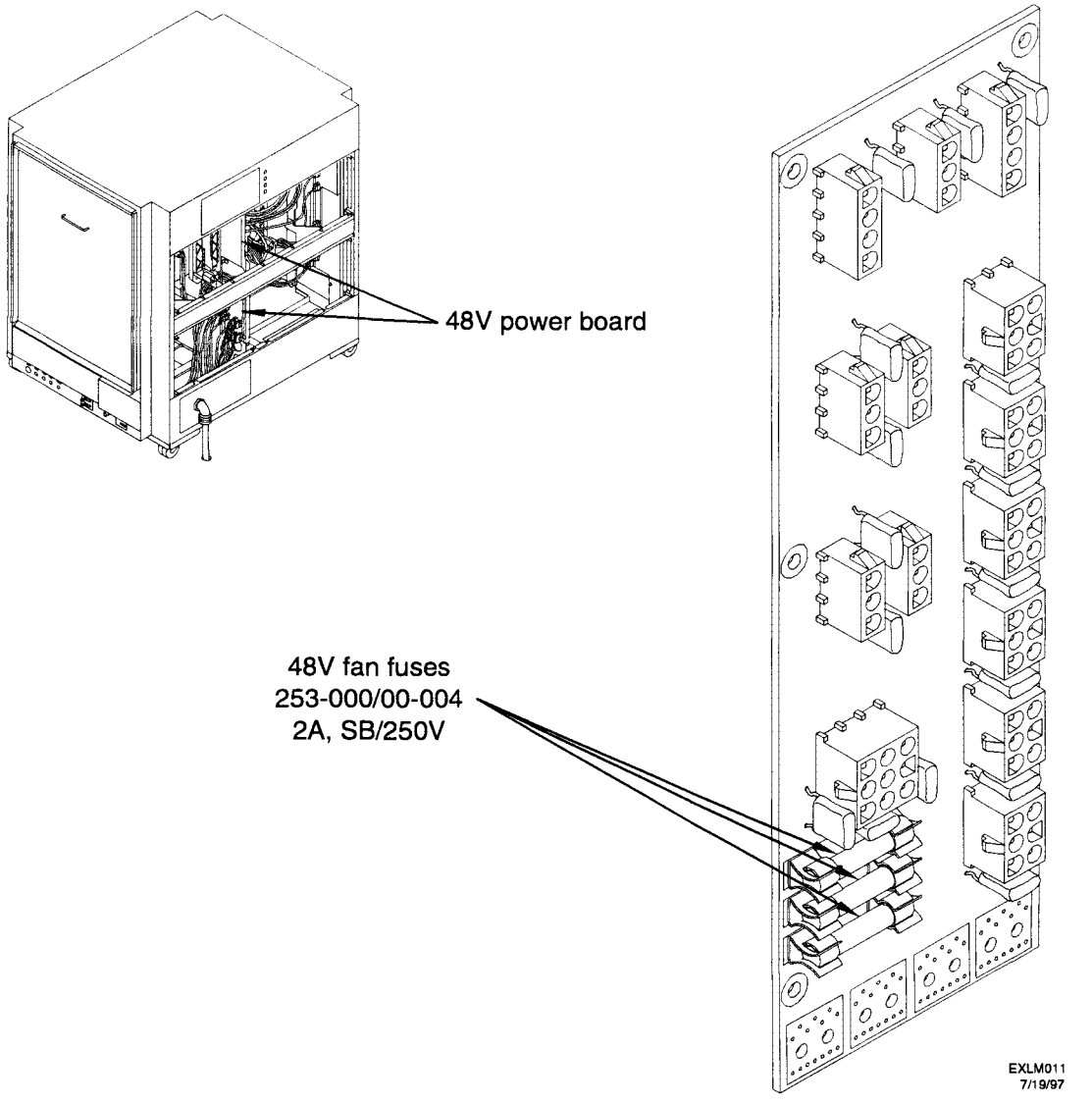


Figure 82 Embedded disk power board fuse locations

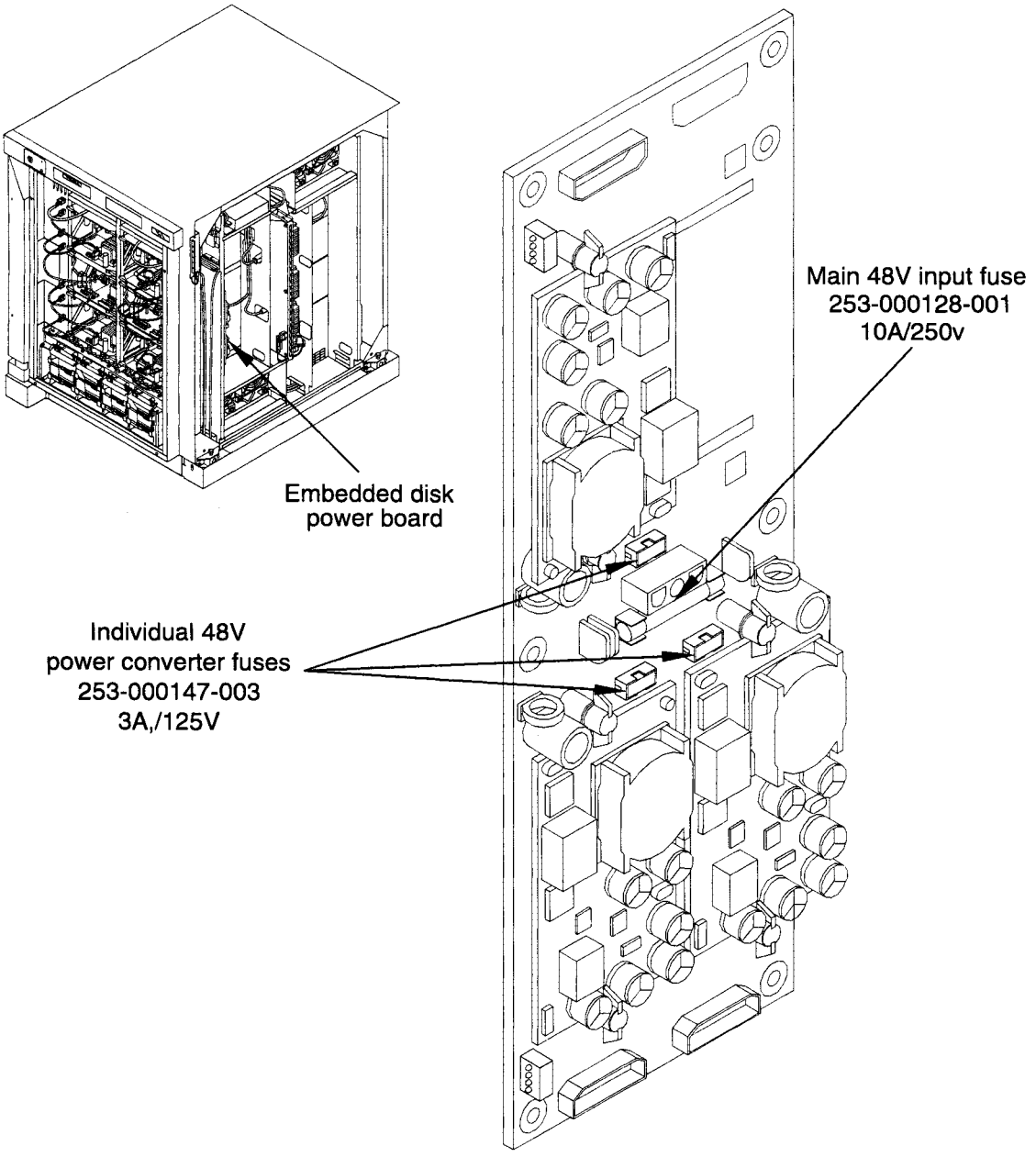
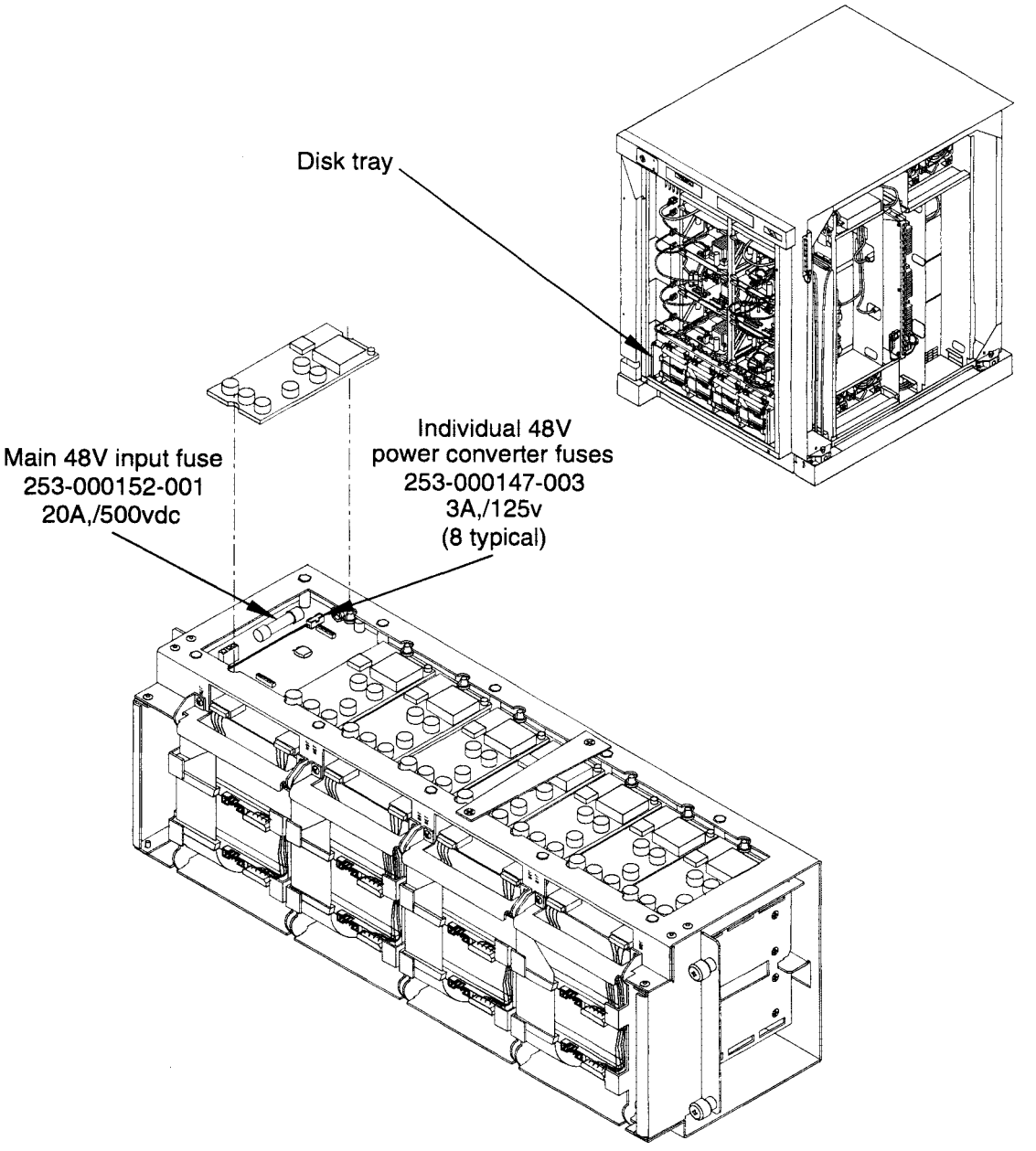


Figure 83 Disk tray power board fuse locations



Note: Always replace fuse when dc to dc converter board is replaced.

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Test point locations

B

General

Test points are invaluable in troubleshooting the system. This appendix identifies and locates all the system test points.

Test point identification

Table 32 identifies the voltages that are associated with the various test points. Figure 84 through Figure 94 shows the location of the system test points.

Table 32 Test point data

Test point	Value	Locations	Allowable readings[1]
VDD	**+3.3 Vdc**	EPB, EMBPB, ENRBPB, ECUB, EIOB	3.23 to 3.36 Vdc
VDDQ	**+1.5 Vdc**	EPB	1.42 to 1.58 Vdc
NEG1R9	**-1.9 Vdc**	EPB	-1.8 to -2.0 Vdc
VCC	**+5 Vdc**	EIOB, ECUB	4.9 to 5.08 Vdc
POS12	**+12 Vdc**	EIOB, ECUB, any disk power module	11.6 to 12.6 Vdc
NEG12	**-12 Vdc**	EIOB	-11.4 to -12.6 Vdc
48V	**+48 Vdc**	All 48V board connectors	45.6 to 50.4 Vdc
POS5	**+5 Vdc**	All disk power modules	4.85 to 5.25 Vdc
48 V power supplies (NPS) output current		48 V power supplies	1 Vdc = 100% = 41.7 A
IMON (current monitor)		All labeled current monitors	66 mv per 1 Adc Example 2 V = 30.3 A

1 Readings shown are not applicable when margining voltages.

Figure 84 Memory power board (EMBPB) test points

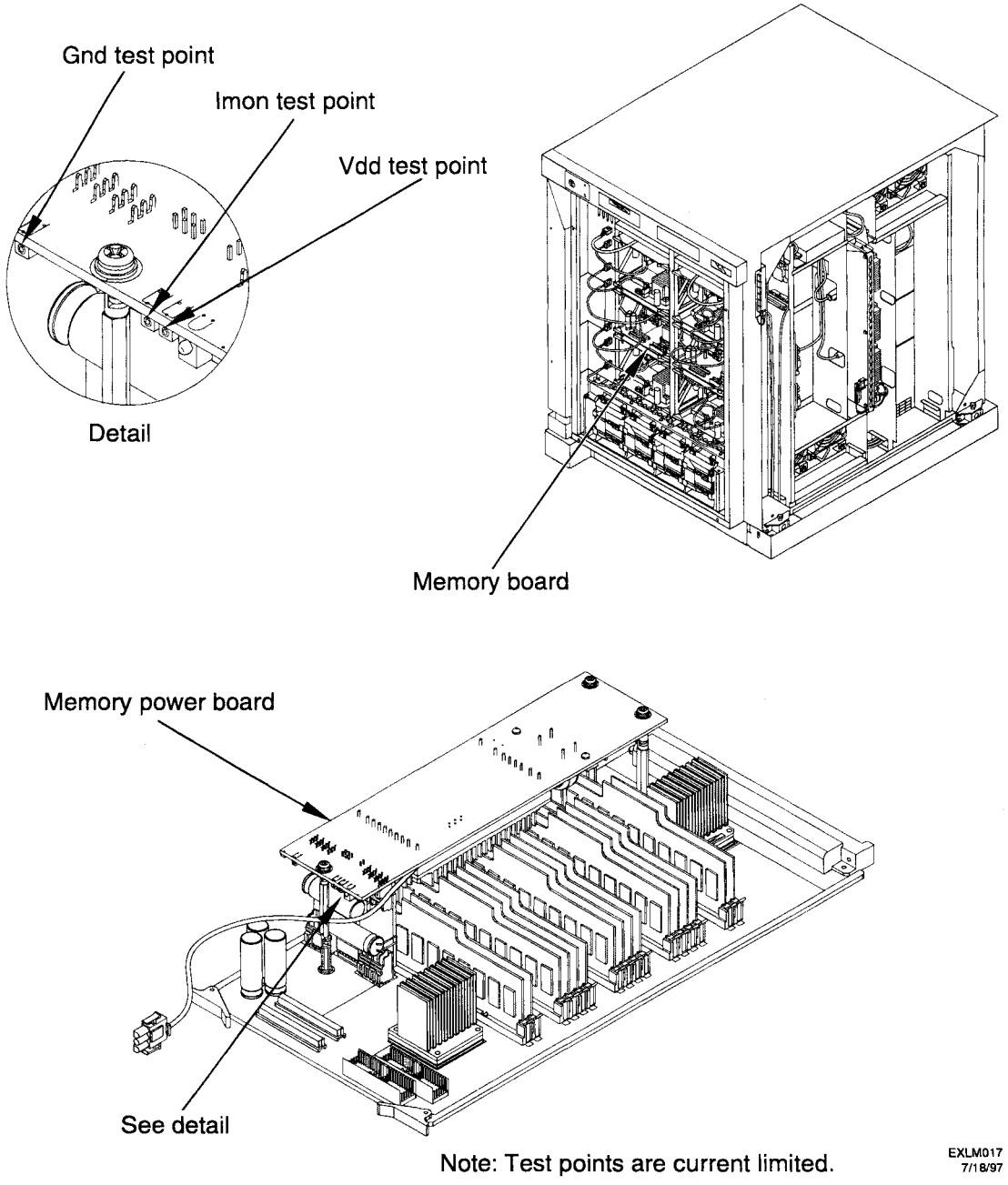


Figure 85 Processor board (EPB) test points

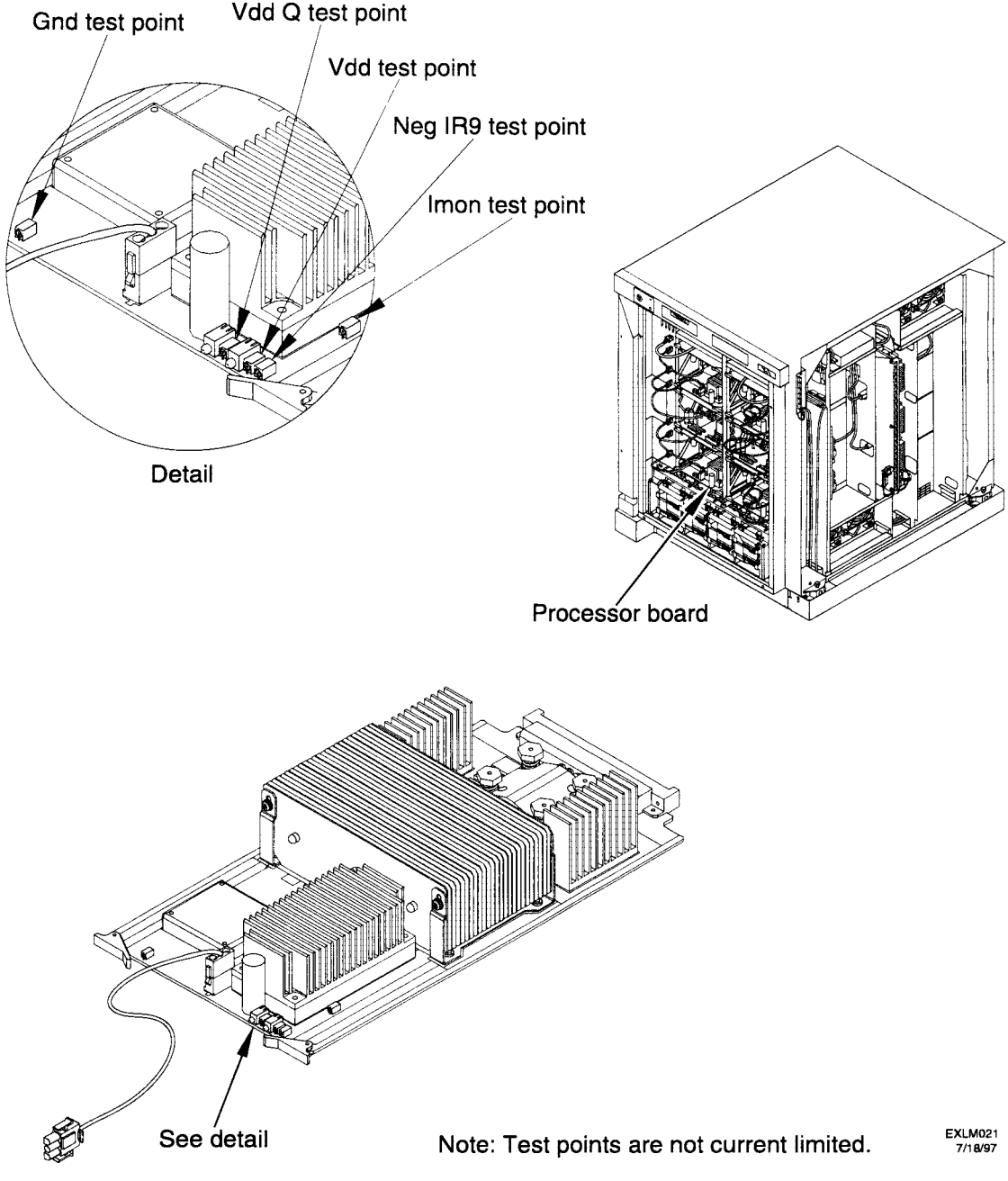


Figure 86 48 volt power supply (NPS) test points

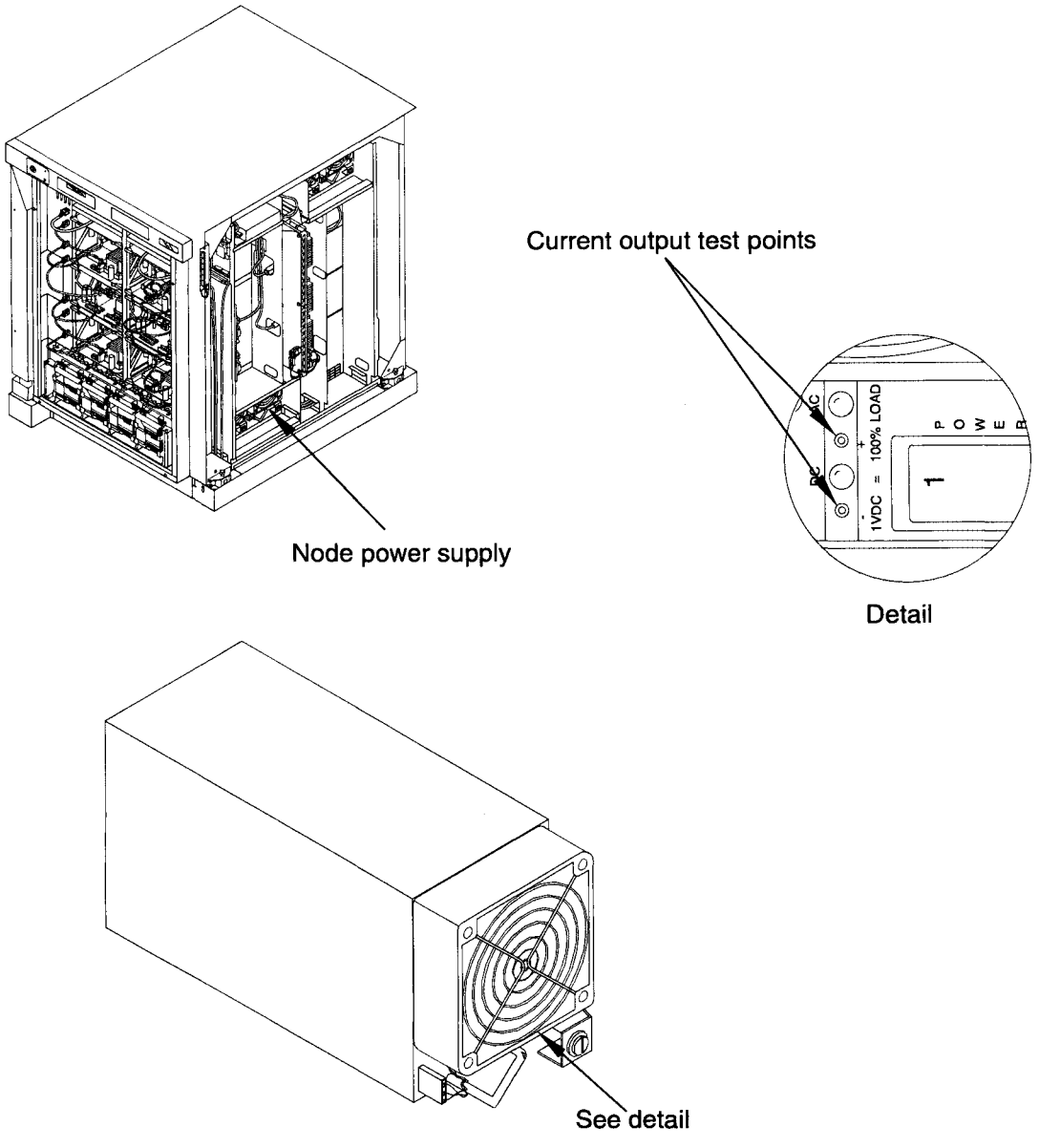


Figure 87 48 volt power suppy (NPS) redundancy switch

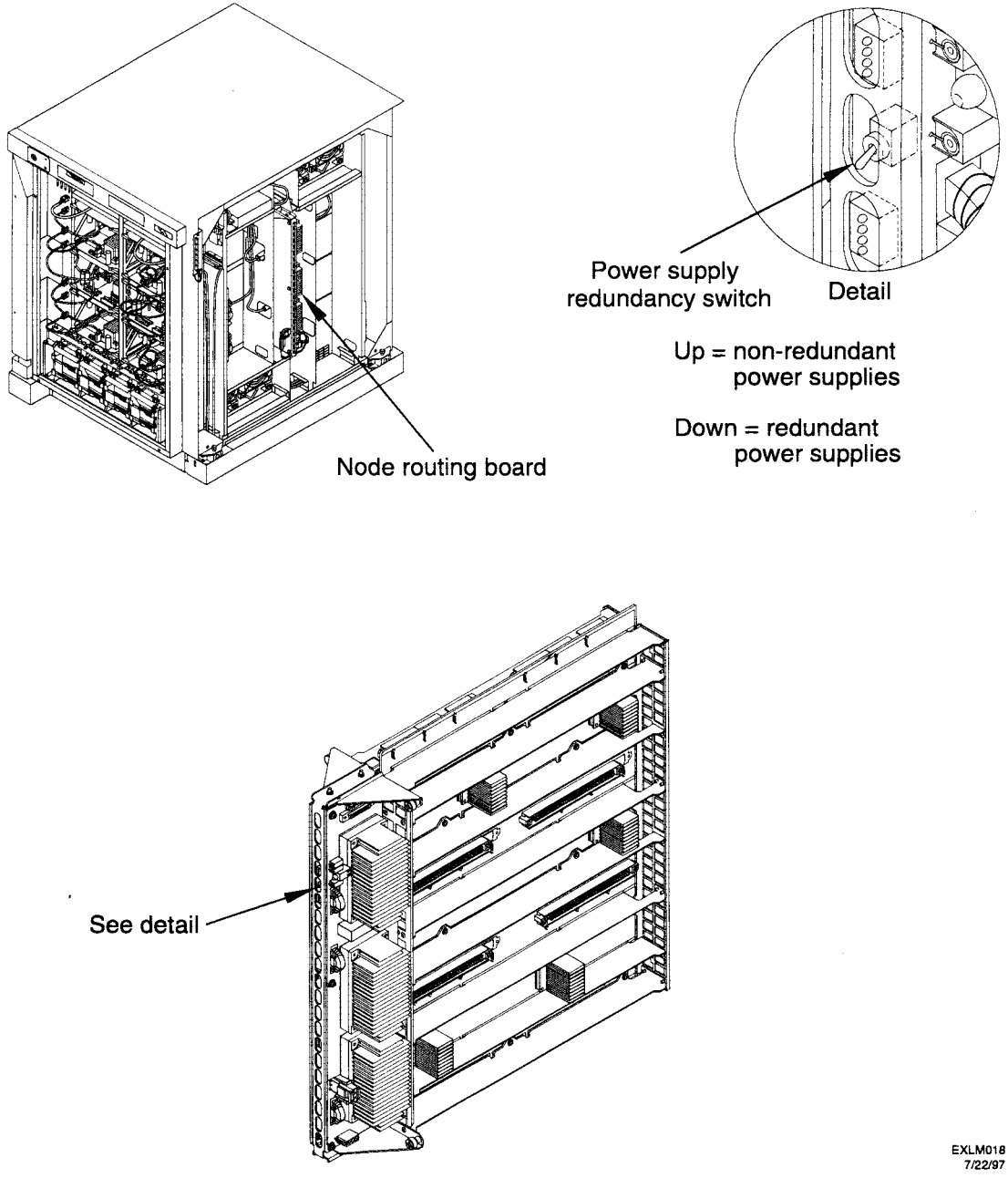


Figure 88 I/O board (EIOB) test points

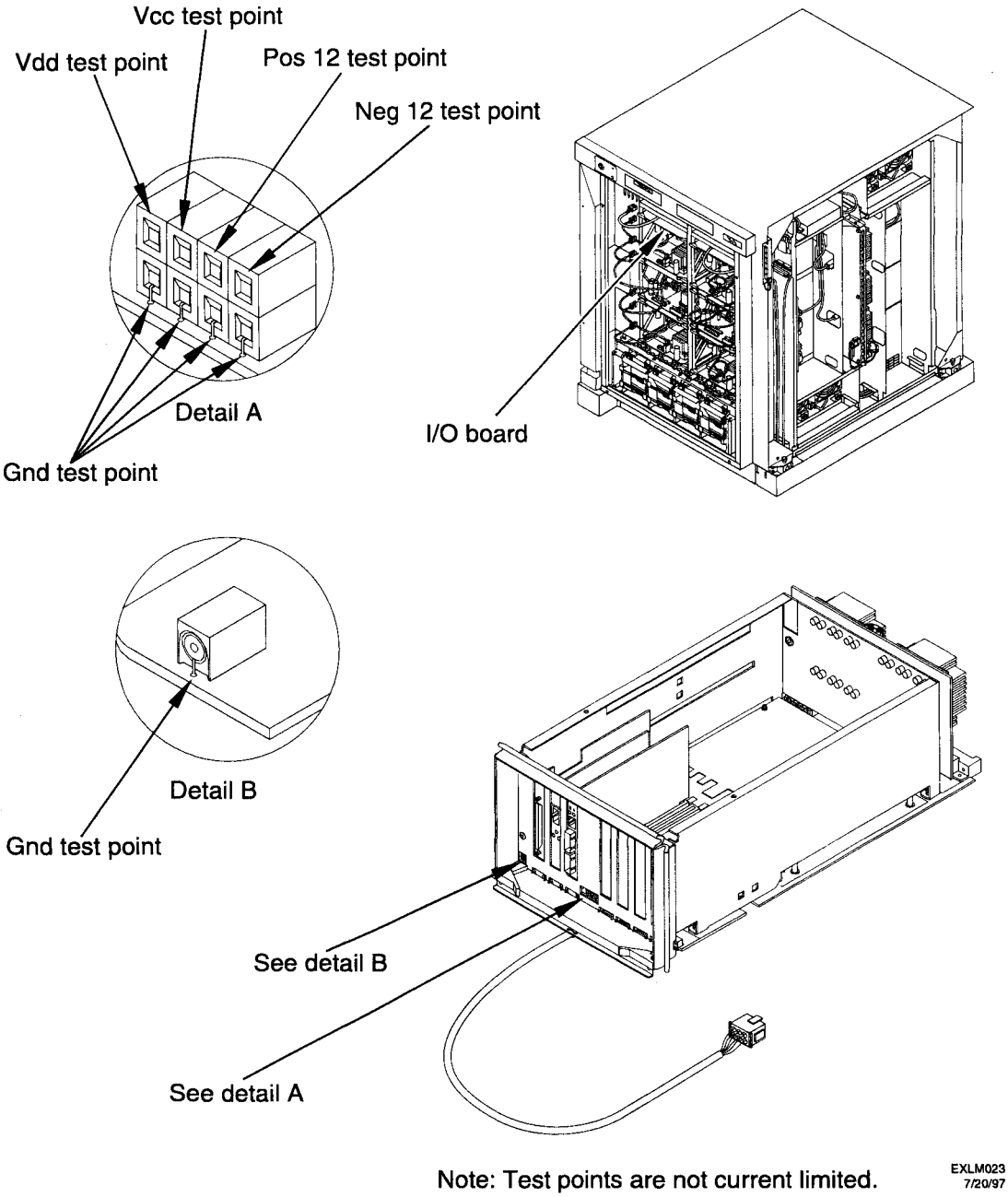


Figure 89 Node routing board power board (ENRBPB) test points

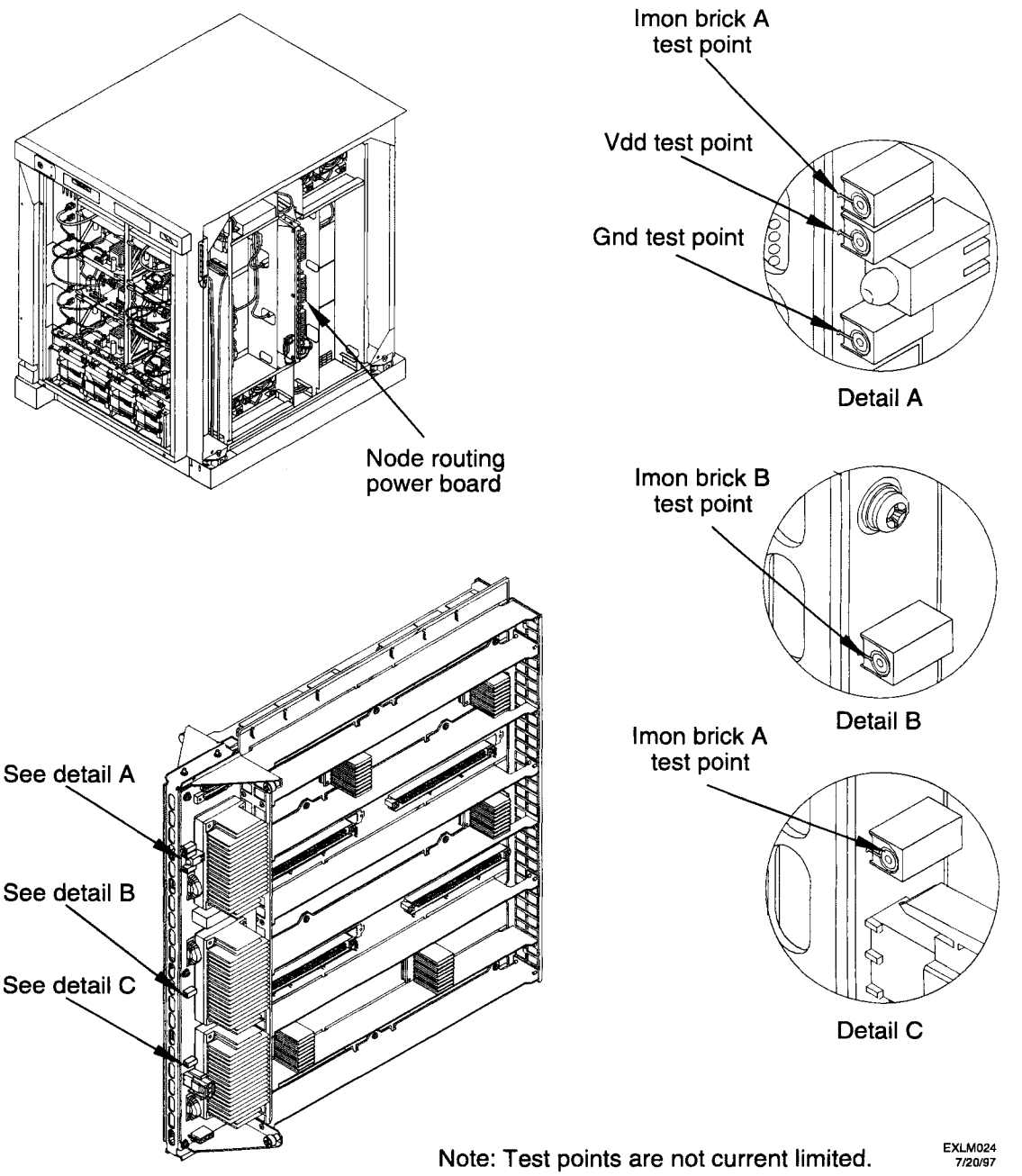
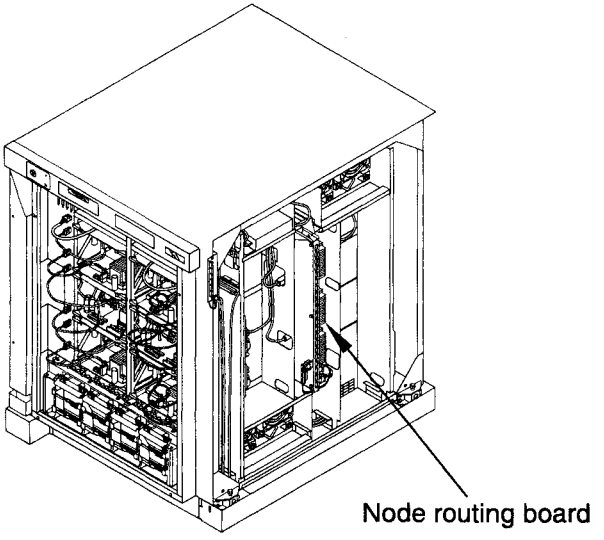
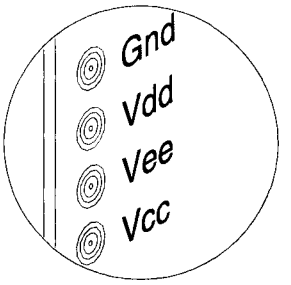


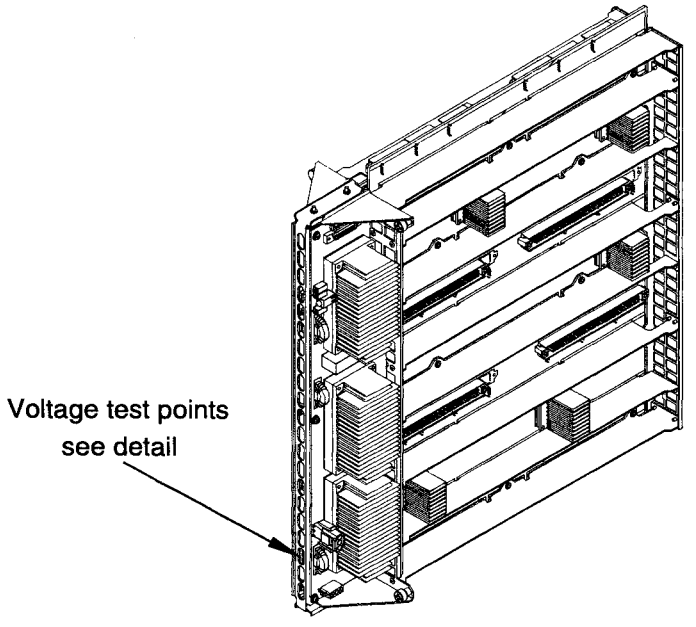
Figure 90 Core utilities board (ECUB) test points





Detail

Test points located on back of ECUB



Note: Test points are current limited.

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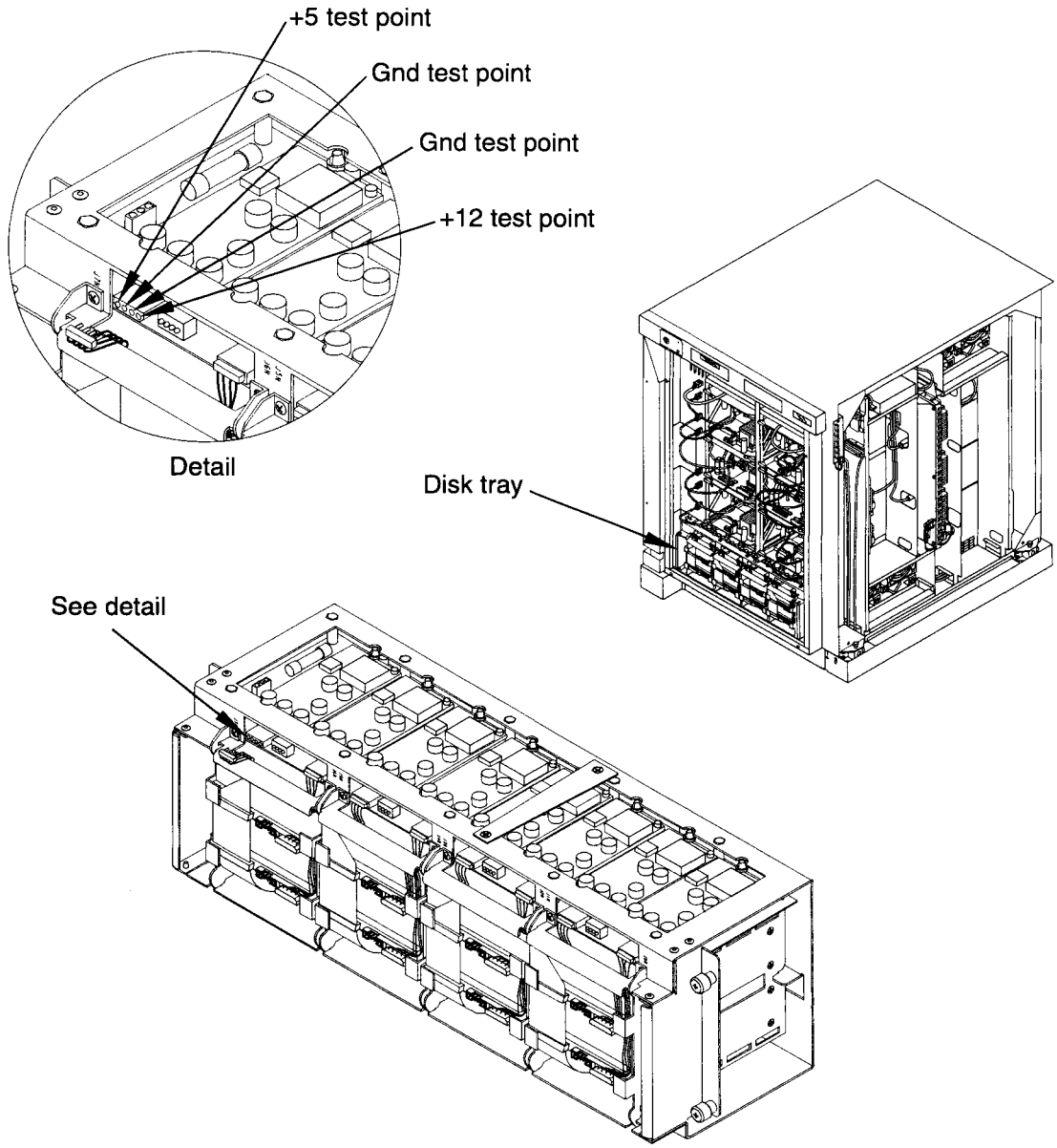
Figure 91 Disk power module test points



Note: If endcap is removed from cable connector, voltages can be probed.
Test points are not current limited.

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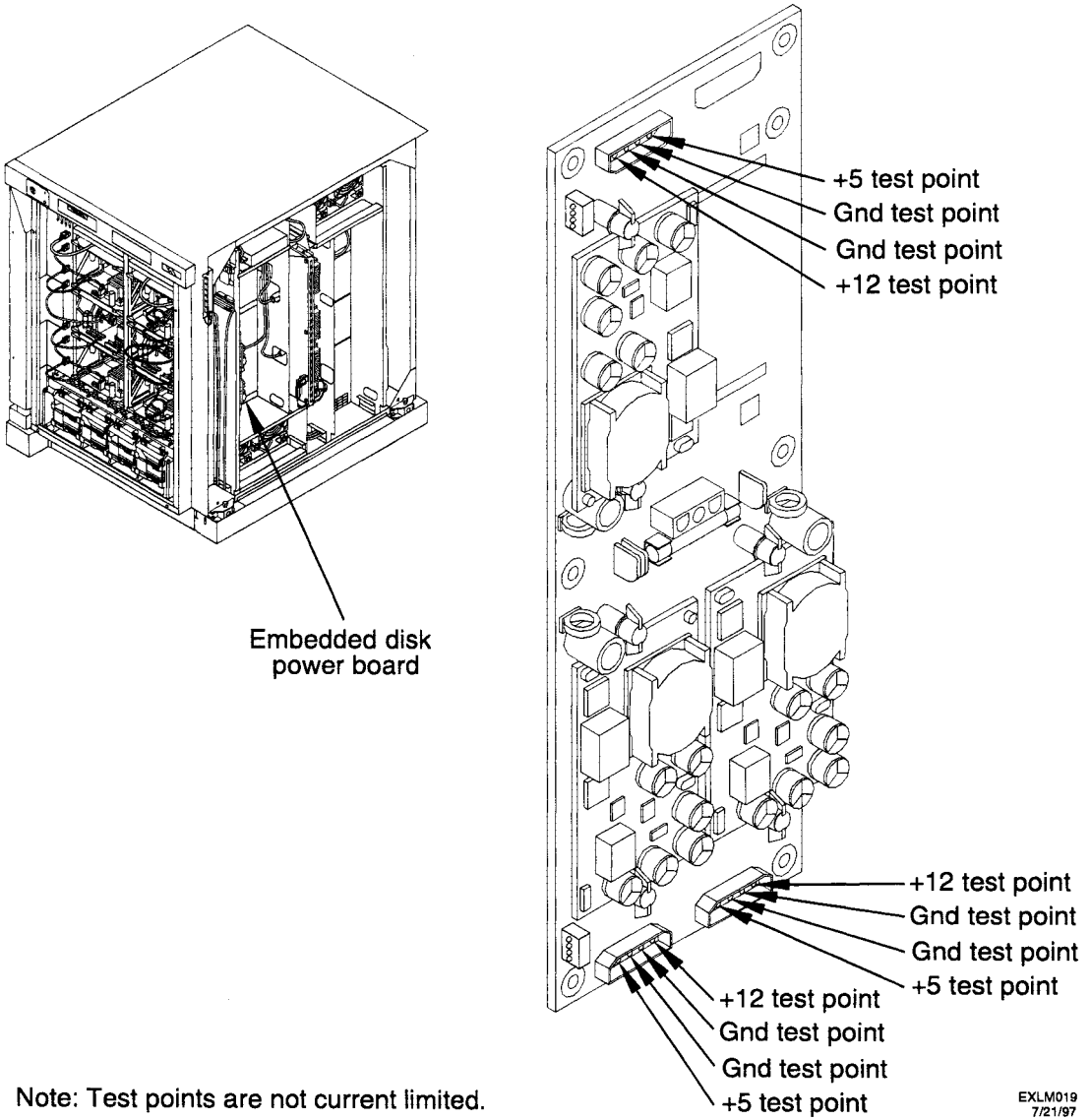
Figure 92 Embedded disk power board test points



Note: Test points are not current limited.

Figure 93 Embedded disk power board module identification

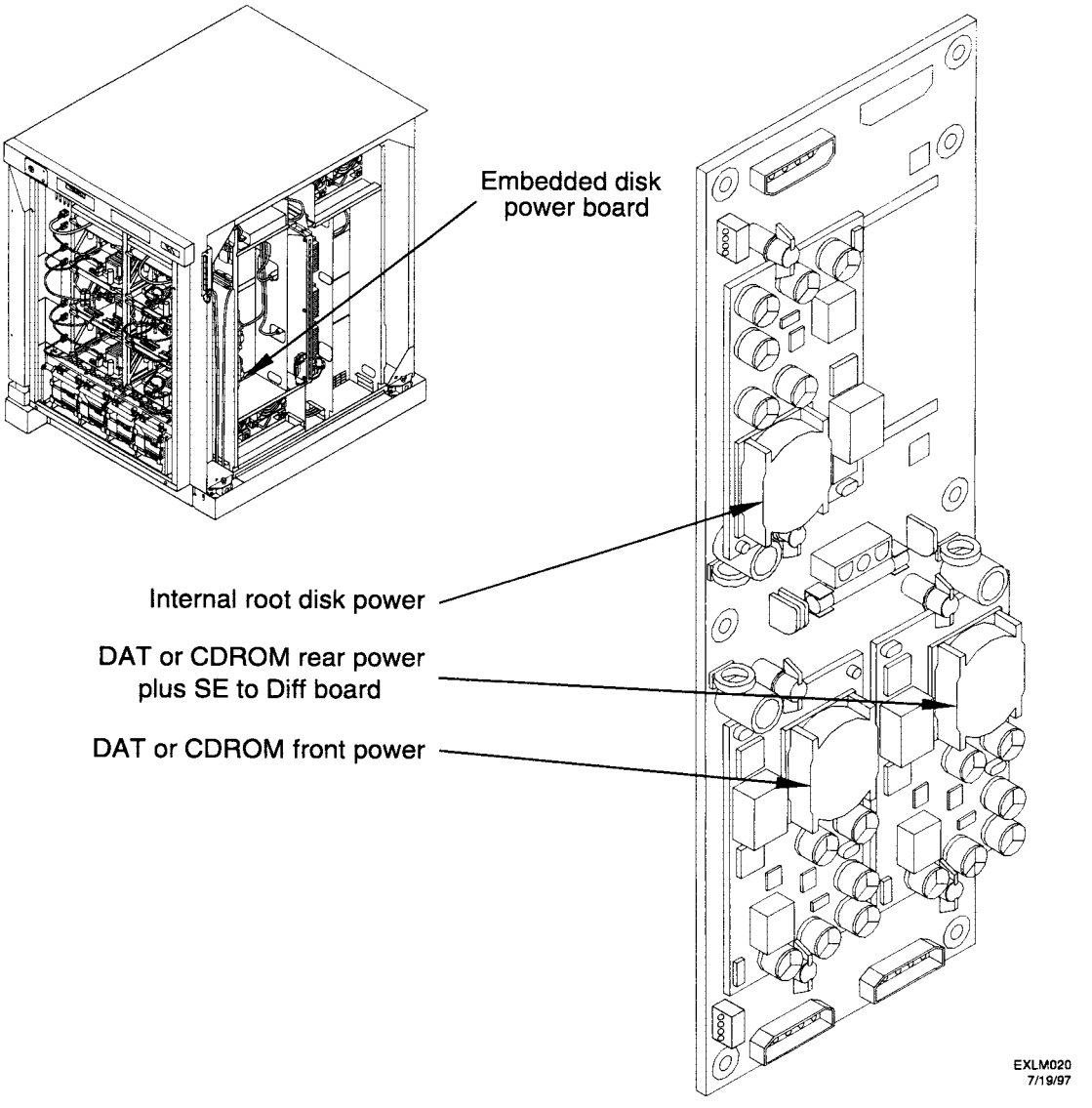
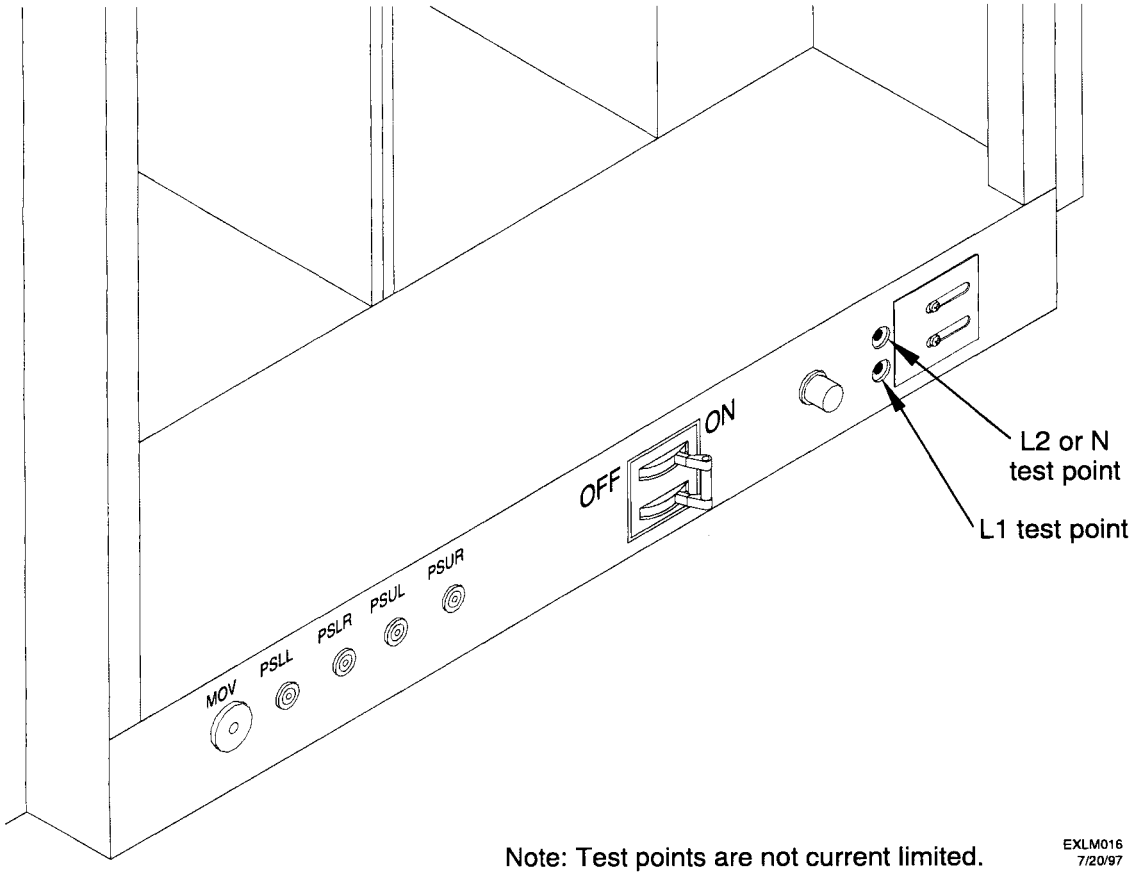


Figure 94 Input power test point



Note: Test points are not current limited.

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